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Control of a Single-Phase Islanded Microgrid Based on Virtual Oscillator Control Enhanced With Power Limitation and Robust Distributed Secondary Control

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ABSTRACT Virtual oscillator control (VOC) has emerged as an alternative solution for controlling parallel connected inverters in microgrids (MGs) due to its self-synchronization and advanced control capabilities. To enhance the operations of VOC-based inverters, this article implements a power limitation controller that dispatches power according to the operating conditions and the primary source availability. Therefore, this mechanism allows the inverter to adapt to the intermittent nature of renewable energy sources and the operational constraints of batteries. The controller can limit both active and reactive power to specified setpoints. When an inverter reaches its power limit, the others that are not restricted by the power limitation take on the extra load. On top of VOC, a robust distributed secondary control was developed to restore the MG voltage and frequency. The controller uses the local frequency and voltage and the powers from the neighboring nodes obtained through a sparse communication network. Last, as part of a single-phase MG configuration, single-phase inverters generate a second-order current component in their dc-link that needs to be restricted from flowing to the dc source. To address this issue, this article implements a minimalist active power decoupling method adapted to the VOC inverter. Extensive simulations and experiments were conducted to validate the operation of the proposed system.

INDEX TERMS Active power decoupling (APD), microgrid (MG), power limitation, secondary control, virtual oscillator control (VOC).

I. INTRODUCTION

The global energy landscape is undergoing a major paradigm shift from traditional synchronous machine-dominated power systems to converter-dominated power systems [1]. The shift to inverter-based resources, such as photovoltaic (PV), wind, and batteries, is largely influenced by the need to adopt sustainable clean energy to meet increasing energy needs. The transition to a more resilient and decentralized power system can be facilitated by microgrids (MGs) [2], [3]. MGs aggregate various distributed energy resources and loads into a controllable unit, capable of operating either standalone or connected to another grid. Several key benefits can be derived from MGs, including improved energy security, reliability, sustainability, and reducing carbon emissions [4]. At the same time, stability challenges are more acute in MGs because of the weak nature of these systems [5]. As a result, more research should be directed primarily toward developing control algorithms that ensure stable and efficient coordinated operation of various distributed energy resources.

Currently, a large percentage of inverter-based resources are controlled through a grid following (GFL) converter [6], which works well when connected to a stiff grid. The GFL controller controls the inverter to behave as a current source in the subtransient time frame. During operation, the inverter must maintain synchronization with the grid through a phase-locked loop (PLL). The need for a voltage source to synchronize with poses challenges for GFL controllers, particularly in weak grids, or during system splits. Furthermore, these GFL inverters are unable to participate in processes such as black start in the event of a total or partial grid shutdown.

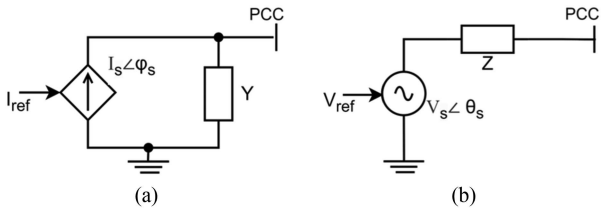

FIGURE 1. Basic inverter models for the two modes of operation: (a) GFL and (b) GFM.

As the landscape transitions toward more decentralized energy generation, grid-forming (GFM) control has emerged as a key enabling technology to overcome the challenges mentioned above [7]. The GFM controller controls the inverter to behave as a voltage source in the subtransient time frame, and it autonomously establishes the inverter's internal voltage and phase angle. GFM controller uses power/current based synchronization and tends to be relatively stable in weak grids due to its nonreliance on PLL to remain synchronized with the rest of the network. Adopting GFM control enhances the stability and reliability of the MG [8]. In addition, GFM can provide other ancillary services, such as black start capability. Models for GFL and GFM controllers are shown in Fig. 1(a) and (b), respectively. Different MG synchronization methods have been proposed in the literature that include PLL-based [9], enhanced PLL [10], consensus based [11], fuzzy logic [12], and non-PLL [13]. As the GFM controllers are gaining attention, the trend has been to replace the PLL with more robust synchronization methods particularly in weak grids where PLL can be unstable [14].

For controlling and managing MGs, a hierarchical control structure consisting of the primary, secondary, and tertiary layers is widely adopted, with each layer having its own control objectives [15]. The dynamics of these layers are decoupled from each other by having different control bandwidths or timescales. The primary layer serves as the basis layer, mainly responsible for regulating voltage and frequency as well as ensuring power sharing. The main GFM controllers discussed in the literature are the droop control, the virtual synchronous machine (VSM), and, more recently, the virtual oscillator controller (VOC) [16]. While the first two techniques are derived from the operation of conventional generators, VOC is based on the dynamics of a nonlinear oscillator, which inherently provides synchronism when coupled within a network. Weakly nonlinear oscillators synchronize to a steady-state sinusoidal limit cycle from an arbitrary initial condition. A comparison between droop control and VOC is provided in [17] where it was shown that VOC provides relatively faster and damped response. To achieve power synchronism, droop control operates on phasor quantities, i.e., active and reactive powers, and the use of low-pass filters on the power loops impacts its dynamic performance. Despite being nonlinear, it was shown in [18] and [19] that VOC subsumes droop in the steady state, but is superior in the transient regime due to its faster synchronization speed. Several oscillator models have been studied in the literature which include the dead zone, Van der Pol, Andronov–Hopf, and dispatchable VOC [20], [21], [22]. This article implements a Van der Pol oscillator for the primary control of the MG inverters. The challenge with the Van der Pol oscillator is the presence of the third harmonic due to the nonlinear voltage dependent current source. In [23], a method is presented that reshapes the nonlinear current source of the VOC, eliminating the third-order harmonic in the output voltage. This method offers faster synchronization in islanded mode compared to the use of a notch filter [24]. Various research has focused on improving the dispatchability of VOC controlled inverters to regulate active and reactive power. In [25], an MG structure consisting of both dispatchable and uncontrolled inverters acting as a slack bus was presented. A complex parameter was introduced in [26] to control the active and reactive power for VOC based inverters in grid connected mode. While these controllers enforce the power supplied by the inverter, this article develops a power limitation strategy for VOC-based inverters, making it more suitable for islanded MGs. In this strategy, the limitation is enabled only when the power being drawn from the inverter tends to exceed its power limit. Enforcing power limitations on each inverter according to its operating conditions provides a way to manage the intermittent nature of renewable energy sources such as PV or wind, and the power constraints of other primary sources like the battery energy system. Power limits ensure that each converter provides power to the load depending on the energy available in the primary source. In addition, these limits can also protect against the load drawing more power than the rated capacity of the converter. Power limitations have been implemented for droop-based control in CERTS MGs testbed to prevent inverter overloading [27], [28]. In this article, a new power limitation control approach is adapted for VOC-based inverters.

The secondary control layer operates on top of the primary control layer. Its objective is to restore the voltage and frequency following the steady-state deviations introduced by the primary layer. The secondary control methods are classified into centralized, distributed, and decentralized [29]. Centralized secondary control generally uses a communication infrastructure to communicate the control variables of all units to the centralized secondary controller. The centralized controller then returns the corrective term to each MG unit. As a result, this control method is highly dependent on the communication infrastructure and is also vulnerable to a single point of failure [30]. Distributed secondary control (DSC) uses local information as well as information received from neighboring units. A sparse network architecture can be adopted to reduce the bandwidth of the network. The two most popular approaches are distributed averaging and the consensus approach [31], [32]. A consensus approach was implemented in [33] for frequency control, which uses linear optimal power flow to dispatch the distributed generators. Additionally, there has been a considerable interest in incorporating artificial intelligence into DSC. To achieve an optimal DSC, a strategy based on reinforcement learning

was proposed in [34]. The method combines Q-learning and pinning control to achieve self-adaptive control. In [35], a data-driven approach was adopted that directly utilizes the measured data for controller design without the knowledge of the model. Fully decentralized control, where decisions are made fully based on local information, is limited by issues such as clock drifts and its inability to achieve global optimization. Several studies have analyzed the impacts of clock drift highlighting its negative impact on the operation of the secondary controller [36], [37], [38]. In [24], a secondary controller was implemented for VOC controlled inverters based on local integrators. However, this approach faces challenges such as clock drift associated with secondary control when it is implemented using separate digital processors. In this article, a low data-rate DSC with an averaging method was implemented, demonstrating robustness against clock drifts.

A subsequent challenge addressed in this article arises from the single-phase configuration of the MG, which is of interest for small-scale residential systems and involves single-phase inverters. In such inverters, electrolytic capacitors are commonly used in the dc-link to provide passive decoupling of both the low- and high-frequency components. The major drawback of electrolytic capacitors is their limited lifetime, particularly in higher temperature environments, common in PV applications. To enhance both the lifetime and reliability of the inverter, active power decoupling (APD) methods have emerged as a viable solution [39]. These APD methods rely on actively redirecting the low-frequency power oscillations to be processed by an auxiliary circuit or energy storage with a higher utilization factor, while the remaining high-frequency component is processed by the dc-link capacitance [40], [41]. In this way, the required capacitance for the dc-link is minimized, enabling the implementation of an all-film capacitor inverter and thereby improving the inverter's lifetime. This article focuses on a minimalist method that achieves APD without the need of additional semiconductor devices, unlike other methods that require more components [42] and which increases the overall cost of the system. This article aims to deliver the following technical contributions.

1) Development of a power limitations strategy for VOC-based inverters to ensure that the energy is dispatched depending on the availability of the primary source.
2) Development of a robust DSC using a distributed averaging approach to restore the MG frequency and voltage.
3) Implementation of an APD in VOC MG applications to eliminate low frequency oscillations in the inverter dc-link current.
4) Integration of VOC with inner voltage and current controllers to provide better control of the proposed single-phase inverter.

II. SYSTEM STRUCTURE

Fig. 2 shows the structure of the considered islanded MG consisting of three parallel 1-kVA single-phase inverters. The parallel configuration allows for integration of various

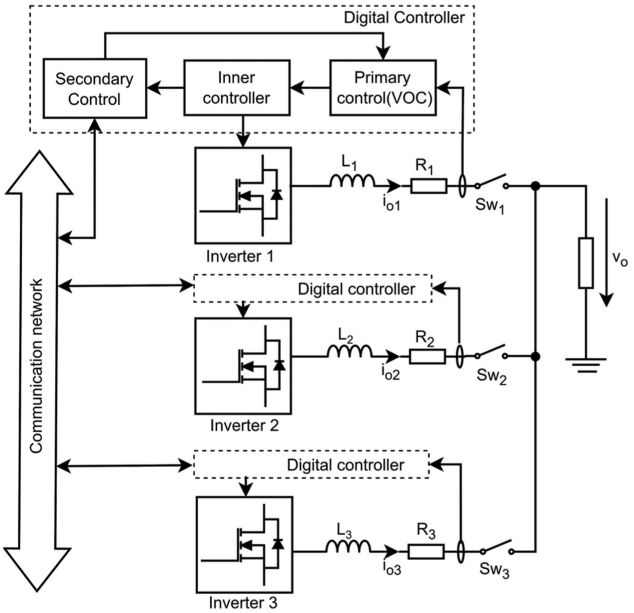

FIGURE 2. Structure of the proposed MG consisting of three parallel inverters.

distributed energy resources that are coordinated to deliver power to a common load. This low-power configuration enables load sharing and is suited for residential applications. Each inverter is connected to the point of common coupling (PCC) through a switch (Sw_i). The series impedance is mainly provided by the inductors L_1, L_2, and L_3 (and their corresponding resistances), which ensure higher order harmonic filtering as well as acting as coupling inductors. The overall structure of each inverter is shown in Fig. 3. Capacitors C_1 and C_2 serve as decoupling capacitors used to implement APD as described later in this article. The primary control is implemented through a VOC-based approach, discussed in the following subsection. On top of the primary layer, a secondary control layer is implemented using a distributed control strategy and a low-bandwidth communication network. The secondary layer provides setpoints to the primary control to achieve the objective of restoring the voltage and frequency, as well as maintaining power sharing.

Fig. 3 shows the overall control structure of one inverter (the others having a similar control), composed of the implemented primary and secondary control layers. The following sections detail each subsystem of the proposed control.

A. VIRTUAL OSCILLATOR CONTROL

As previously discussed, VOC implemented in GFM inverters allows self-synchronization, making it suitable for parallel inverters in MG. In this control strategy, each inverter emulates the dynamics of a nonlinear Van der Pol oscillator. Fig. 4(a) shows a typical model of a Van der Pol oscillator, where $i_{o(i)}$ is the sensed feedback current from the inverter and v_{VOC} is the oscillator output voltage. The structure is composed of a resonant tank LC circuit that establishes the system frequency,

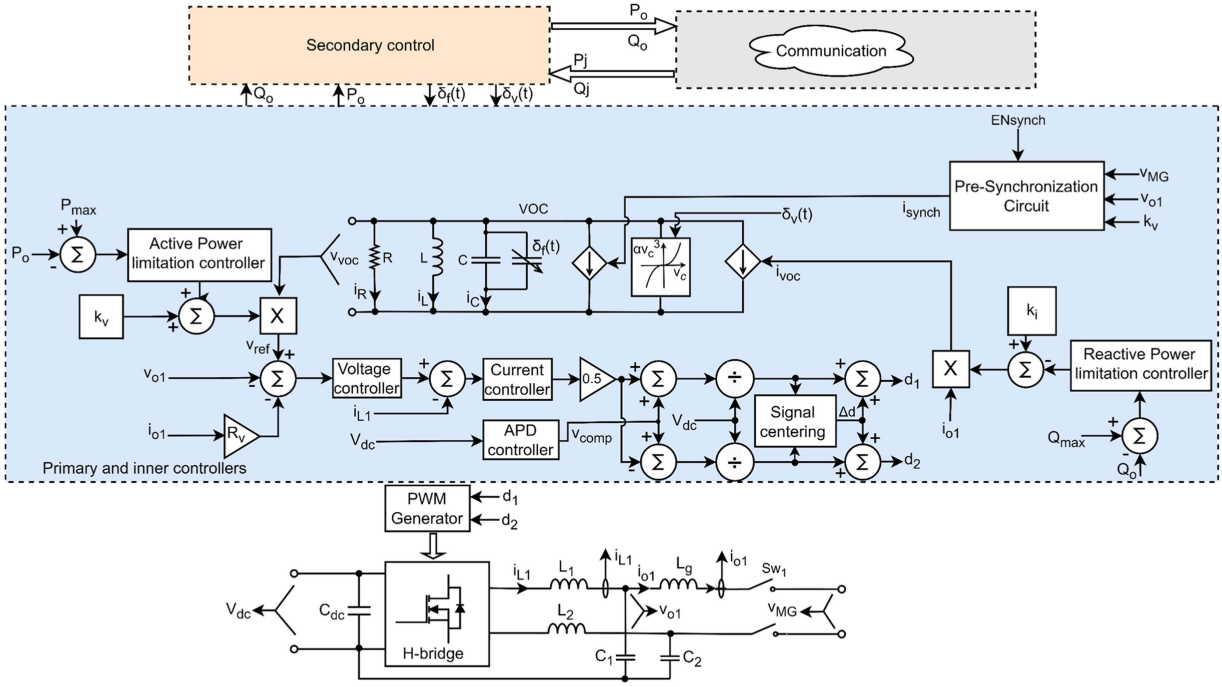

FIGURE 3. Overall control structure of one inverter with primary and secondary control loops.

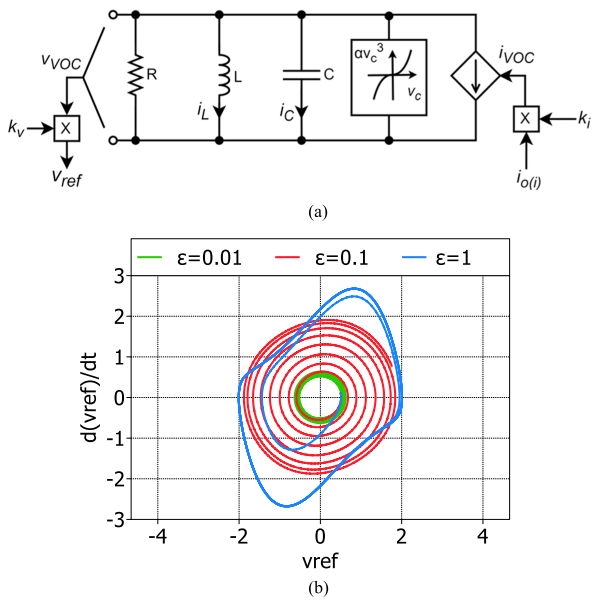

FIGURE 4. VOC based on van der pol oscillator: (a) circuit representation and (b) phase portrait of the steady-state limit cycles.

a nonlinear voltage-dependent current source, and a damping resistance. The VOC dynamics are given by the following equations [21]:

$$L\frac{di_L}{dt} = \frac{v_{\text{ref}}}{k_v} \tag{1}$$

$$C\frac{dv_{\text{ref}}}{dt} = -\alpha\,\frac{v_{\text{ref}}^3}{k_v^2} + \sigma v_{\text{ref}} - k_v i_L - k_v k_i i_{o(i)} \tag{2}$$

where L and C are the virtual inductance and capacitance, respectively.

The parameters α and σ are the voltage regulation parameters. The interface between VOC and the inverter is achieved through the current gain k_i and the voltage gain k_v. The gain k_i is added with the output of the reactive power limitation controller, while k_v is added with the output of the active power limitation controller. This mechanism enables active and reactive power limitation, as will be described in subsection D. A detailed design of VOC parameters is provided in [21].

Being a weakly nonlinear controller, VOC stabilizes to a sinusoidal limit cycle from any arbitrary initial condition. To understand the dynamics and the limit cycles of an unloaded VOC ($i_{o(i)} = 0$), (1) and (2) can be transformed into a second-order differential equation as follows, assuming the controller is operating in quasi harmonic limit, i.e., ε approaches zero:

$$\ddot{v}_{\text{ref}} - \varepsilon\sigma\left(1 - \beta v_{\text{ref}}^2\right)\dot{v}_{\text{ref}} + v_{\text{ref}} = 0 \tag{3}$$

where $\varepsilon = (L/C)^{1/2}$ and $\beta = 3\alpha/(k_v{}^2\,\sigma)$.

A phase portrait for the trajectory of the Van der Pol oscillator is plotted in Fig. 4(b) for different values of ε with $\beta = 1$. As shown, the oscillations approximate nearly sinusoidal limit cycles as ε approaches zero. However, the smaller the value of ε, the slower the dynamic response.

To generate a reference signal from the Van der Pol oscillator to modulate a single-phase inverter, the output voltage across the VOC capacitor (v_{VOC}) can be used. This yields a steady-state droop characteristic that provides a tradeoff between the active power (P)–voltage (V) and reactive power

(Q)–frequency(ω) as in (4) and (5), which shows VOC averaged dynamics. These steady-state droop characteristics are embedded within the averaged dynamics of the VOC [15]

$$\dot{V} = \frac{\sigma}{2C}\left(V - \frac{\beta}{2}V^3\right) - \frac{k_v k_i}{2CV}P \tag{4}$$

$$\dot{\theta} = \omega^* - \omega + \frac{k_v k_i}{2CV^2}Q \tag{5}$$

where ω^* is the reference frequency and P, Q are the averaged active and reactive output powers of the inverter.

This inverse relationship (i.e., $P - V$, $Q - \omega$) is common in low-voltage networks, where the line impedances are predominantly resistive [43]. An important point to note is that, unlike conventional VOC control, where v_{VOC} is directly used to generate the inverter PWM pulses, in this article we propose adding between the VOC and the PWM generator an inner voltage–current control loop, as shown in Fig. 3. In this case, the oscillator capacitor voltage serves as the reference voltage for the voltage controller. Furthermore, the grid-side current is used as VOC input, instead of the inverter-side current. The reason for using this approach is to control the differential voltage v_{o1} across the inverter capacitors as a voltage source, rather than controlling the inverter terminal voltage. This method offers improved performance, as the decoupling capacitors (C_1 and C_2) shown in Fig. 3 inherently create a larger capacitive load for the inverter compared to a conventional inverter. More details on APD on a differential single-phase inverter are provided in subsection *F*.

B. VOLTAGE AND CURRENT CONTROLLERS

In the conventional implementation, VOC directly controls the inverter voltage, however due to the nature of the adopted topology, this article proposes to use an inner voltage–current control loop to control the inverter, and the VOC as an outer controller, as stated previously. Both controllers are implemented using proportional multiresonant controllers for sinusoidal tracking. The inner current controller is designed to have a higher bandwidth compared to the voltage controller. The advantages of using these controllers are that they can be implemented in the natural reference frame. In addition, they also provide selective lower order harmonic compensation. The transfer functions of the voltage and current controllers are given as follows:

$$G_I(s) = k_{pI} + \sum_{h=1,3,5} \frac{k_{hI}\, s}{s^2 + (h\omega)^2} \tag{6}$$

$$G_V(s) = k_{pV} + \sum_{\substack{h=1,3,5,\\ 2,4}} \frac{k_{hV}\, s}{s^2 + (h\omega)^2} \tag{7}$$

where k_{pI} and k_{pV} are the proportional terms that determine controller dynamics such as bandwidth, gain, and phase margins, while k_{hI} and k_{hV} are the gains of the sinusoidal integrators.

The constant k_{pI} was chosen to be equal to $L/(3T_s)$ [44], where L is the total inverter inductance and T_s is the sampling period. To decouple the dynamics of the outer voltage loop from the inner current loop, k_{pV} was chosen to be 10 times less than k_{pI}.

Besides compensating for the odd harmonics, the voltage controller also includes even harmonics resonators for removing the even harmonics from the output voltage, which may be caused by the APD in practice when the two inverter arms are not perfectly balanced. For practical implementation, the resonant controllers were discretized using an approach based on two discrete integrators [45]. This method has the advantage of being simple and allowing frequency adaptation, where the frequency can be adjusted with the actual measured value in real time, limiting the impacts of frequency mismatch between references and measurements. Furthermore, to provide active damping to the system, a virtual damping resistor R_v was added as shown in Fig. 3.

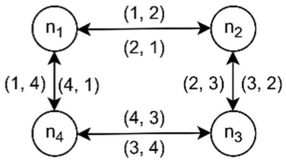

FIGURE 5. Communication graph for inverter nodes.

C. SECONDARY CONTROL

As already mentioned in the introduction, one of the key challenges in implementing decentralized secondary control in real MG applications is the presence of clock drift [46]. Each digital processor used for controlling each inverter uses its own clock to generate time signals. These clocks, which are used to generate time signals, differ slightly from each other, a phenomenon referred to as clock drift. The effect of clock drift is more pronounced in the secondary control layer. As a result, decentralized secondary control with local integrators can regulate the voltage and frequency, however, clock drift causes the powers to diverge over time. Using communication between the inverters can alleviate the effect of clock drift. A communication network can be modeled by an undirected graph with nodes and a set of connections denoted as $G(\upsilon, \xi, A)$ where $\upsilon = \{1, 2, 3 \ \ldots \ n\}$, $\xi = \{(1,2), (2,1), (2,3), (3,2) \ \ldots\}$ and A is a symmetric adjacency matrix that captures the connections between the nodes. A value of one indicates a connection between two nodes, and a value of zero represents no connection. To reduce the complexity of the communication network, a sparse network is considered in this article, where each inverter communicates with two of its nearest neighboring inverters. This reduces the bandwidth requirement, the computational burden as well as the complexity of communication links. When each inverter communicates with all others, the control accuracy improves, but the cost and complexity increase.

Fig. 5 shows an example of a directed graph with $n = 4$.

For this network topology, the adjacency matrix can be defined as follows:

$$A = \begin{bmatrix} 0 & 1 & 0 & 1 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \\ 1 & 0 & 1 & 0 \end{bmatrix}. \tag{8}$$

The proposed secondary controller described by (9) and (10) uses local information and collects data from its immediate neighbors to improve the global optimization performance of the whole MG system and control actions coordination. Through this control, the effects of clock drift on the secondary control are mitigated, as clearly evidenced by experimental measurements shown later. The first term of the proposed secondary frequency controller compares the measured frequency at the PCC to the nominal frequency and the error passed through an integrator. The secondary voltage controller compares the nominal rms voltage to the average of the rms voltages of all inverters. Through this way, the average voltage of all nodes is brought closer to the nominal voltage. This approach helps to solve the conflict between voltage regulation and active power sharing. The second term is generated by each inverter through comparing its normalized power to the average normalized powers of its nearest neighbors. The generated error is also passed through the integrator, and the two terms are combined to generate the compensatory terms. In this way, both frequency and voltage regulation and power sharing are achieved. The averaging of voltages and powers in (9) and (10) occurs each time a new packet containing data from a neighbor inverter arrives through the communication channel. For frequency restoration, the generated compensatory term is added to the virtual capacitance of the VOC as follows: $C_{\text{new}} = C + \delta_f(t)$, where C is the nominal capacitance. In the case of voltage, the generated compensatory term is added to the VOC alpha term as follows: $\alpha_{\text{new}} = \alpha + \delta_v(t)$. The secondary controllers are described as follows:

$$\delta_{f(i)}(t) = k_{If} \int (\omega_0 - \omega_i) dt + k_{IQ} \int \left(\frac{Q_i}{Q_i^*} - \frac{1}{n} \sum_{j=1}^{n} \frac{Q_j}{Q_j^*} \right) dt \tag{9}$$

$$\delta_{V(i)}(t) = k_{IV} \int \left(V_0 - \frac{1}{n+1} \left(V_i + \sum_{j=1}^{n} V_j \right) \right) dt - k_{IP} \int \left(\frac{P_i}{P_i^*} - \frac{1}{n} \sum_{j=1}^{n} \frac{P_j}{P_j^*} \right) dt \tag{10}$$

where k_{If}, k_{IV}, k_{IQ}, and k_{IP} are the integrator gains. $P^*{}_i$ and $Q^*{}_i$ are the rated active and reactive power of the current inverter, while $P^*{}_j$ and $Q^*{}_j$ are the rated active and reactive power of the neighboring inverters. V_o and ω_o are the nominal rms voltage and frequency, respectively.

A low-bandwidth network can be used to communicate the powers to the neighboring nodes. The controller gains are tuned to provide a compromise between the voltage/frequency regulation and power sharing.

While the proposed DSC and the power limitation approaches are effective for managing the operations of the MG, their reliance on communication poses certain limitations from communication delays and failures that may affect system performance. Another challenge is the vulnerability of the network to cyberattacks, therefore, robust security measures will be required to protect the network.

The adopted sparse communication network allows for the system to be scalable in real-world applications by reducing the bandwidth and the network complexity. Furthermore, distributed control also reduces computational burdens associated with centralized controllers. Being based on single-phase inverters, the proposed MG is suitable for kW-range applications. The solution can be expanded to higher power applications using three-phase inverters.

1) SECONDARY CONTROLLER TUNING

For tuning the secondary control parameters, a reduced model was derived that neglects the electrical dynamics with a time constant less than one ac cycle, thus employing rms values. The basic criterion of the secondary controller tuning is to ensure decoupling of the primary control by ensuring it operates at a much lower time scale. In this context, a simplification assumption that neglects the dynamics of the inner current and voltage controllers was considered. The VOC behavior is defined by the rms voltage and phase according to (4) and (5). The secondary control loops, defined by (9) and (10), interact with the VOC by adjusting the parameters α and C to restore voltage and frequency, as described in the previous subsection.

The optimal parameters of the secondary voltage and frequency control ($k_{IV} = 0.05$ A/(V4.s) and $k_{If} = 0.002$ F/rad) were selected based on the targeted response time relative to the primary control. The response time of the primary controller (i.e., VOC) was determined following a step change in the load from zero to nominal. The voltage settling time of the primary control, t_p, was defined as the time elapsed between the disturbance and when the voltage enters 0.5 V deadband around the steady-state value. A deadband of 0.05 Hz was considered for frequency. Next, the gain of the secondary voltage controller (k_{IV}) was varied, and the voltage restoration time (t_{sV}) was calculated relative to t_p. The results are shown in Fig. 6. To ensure decoupling the secondary and primary control levels, k_{IV} was chosen such that the secondary control is at least ten times slower than the primary control. With these conditions, Fig. 6 shows that the gain of the secondary control loop (k_{IV}) should be less than 0.055 A/(V^4.s). However, smaller values of k_{IV} result in a secondary controller being too slow.

For the secondary frequency control, a slower dynamic was imposed to ensure decoupling between the voltage and frequency restoration loops. Fig. 7 shows the frequency time

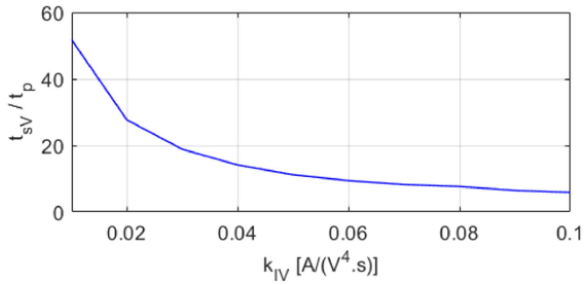

FIGURE 6. Time response of the voltage secondary control normalized to the time response of the primary control.

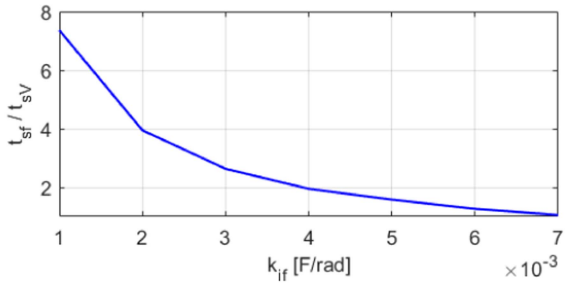

FIGURE 7. Secondary control frequency time response normalized to the voltage time response.

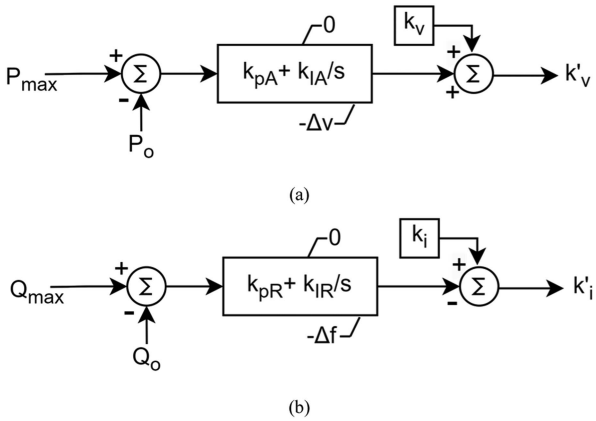

FIGURE 8. Power limitation: (a) active power and (b) reactive power.

response t_{sf} of the secondary control, normalized to the previously defined voltage restoration time ($t_{sV} = 0.05$s), as the gain of the secondary frequency controller (k_{If}) varies within a suitable range. The optimal value of k_{If} was chosen to be 0.002 F/rad, which gives a ratio between the time constants (t_{sf}/t_{sV}) of around four.

D. POWER LIMITATION

The proposed power limitation controllers shown in Fig. 8(a) and (b) can limit both the active power and the reactive power provided by each inverter. The values $P_{\max}/Q_{\max}$ set the limits of the active/reactive power on each inverter according to its operating conditions. These limits are compared to the measured output powers, and the errors fed to an integrator. It is important to note that the upper saturation limits for the integrators are zero, implying that the integrator produces an output only when measured P_o/Q_o become greater than $P_{\max}/Q_{\max}$, respectively.

The outputs of the power limitation controllers are added to the VOC parameters k_v and k_i. By this way, the VOC parameters are adjusted, resulting in a change of the active and reactive powers shared by the inverter. Consequently, the other inverters that have more capacity will supply more power to balance the load consumption. The maximum active power ($P_{\max}$) that an inverter can supply is determined by the available power from the primary source. The maximum reactive power ($Q_{\max}$) is typically given by the remaining capacity of the inverter. It is important to note that while this article presents a method for controlling active and reactive power, determining $P_{\max}$ and $Q_{\max}$ based on the primary source operation is beyond the scope of this article.

TABLE 1. System Parameters

kpA	0.001	0.02	0.05	0.1	0.2
$ts[ms]$	100	50	90	100	∞

TABLE 2. Settling Times for Different Values of k_{IA}

k_{IA}	1	3	5
$t_s[ms]$	90	55	65

1) PARAMETER TUNING FOR ACTIVE AND REACTIVE POWER LIMITATION

Both the proportional and the intergrator constants of the power limitation controllers shown in Fig. 8 were tuned to minimize the response time. To exemplify how the time response can be identified, a step change in the load of 1 kW was introduced while one of the three inverters having a power limitation ($P_{\max} = 0.2$ kW). The settling time (t_s) was defined as the time elapsing between the load change and the time the power delivered by the limiting inverter settles settles within the range of $\pm 5\%$ of $P_{\max}$. Initially, the proportional constant k_{pA} is varied while the integral constant k_{IA} is mantained constant at its optimal value. Fig. 9(a) shows the system response in terms of active powers of the three inverters as k_{pA} is varried, while Table 1 shows the settling times. The optimum value of k_{pA} was found to be around 0.02, where the settling time is at minimum (50 ms). It is important to note that the response time is also affected by the power measurement where the power calculation needs to be averaged over one ac cycle. Similarly, the integrator of the controller is tuned by varying k_{IA} while keeping the proportional term to the optimal value previously defined. Fig. 9(b) shows the system response and Table II shows the settling times. In this case, the integral constant was chosen to be 3 with a minimum settling time of 55 ms.

A similar approach was also followed to find the optimum gains of the reactive power limitation controller. A step

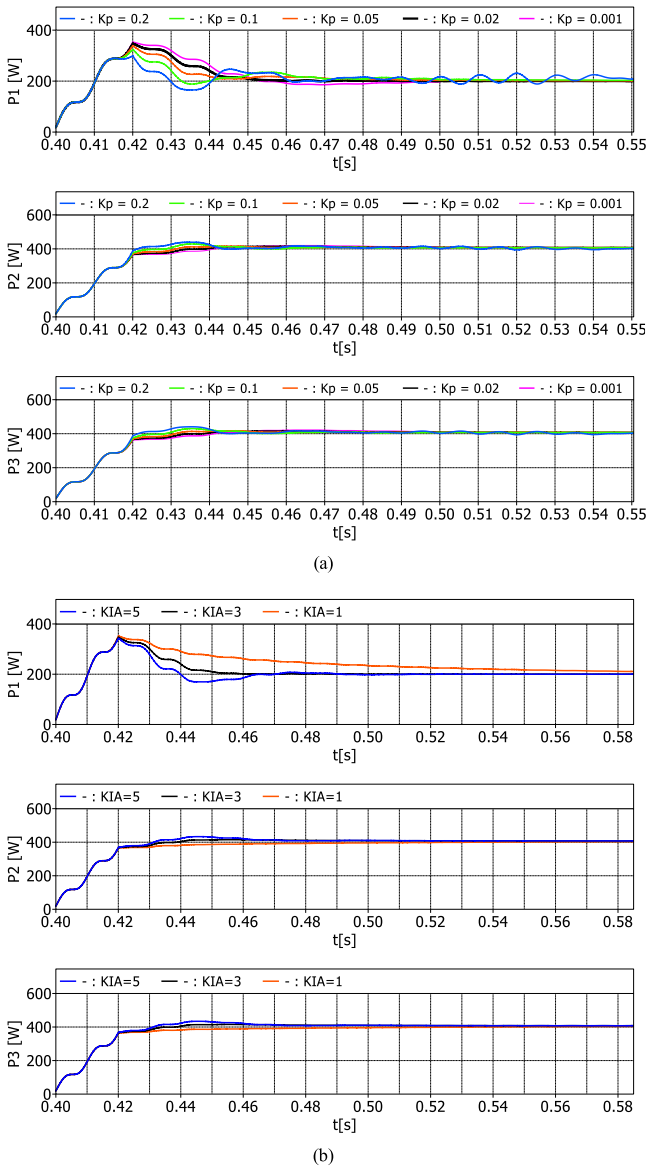

FIGURE 9. Active power limitation dynamics (a) varying k_{pA} mantaining k_{IA} constant and (b) varying k_{IA} mantaining k_{pA} constant.

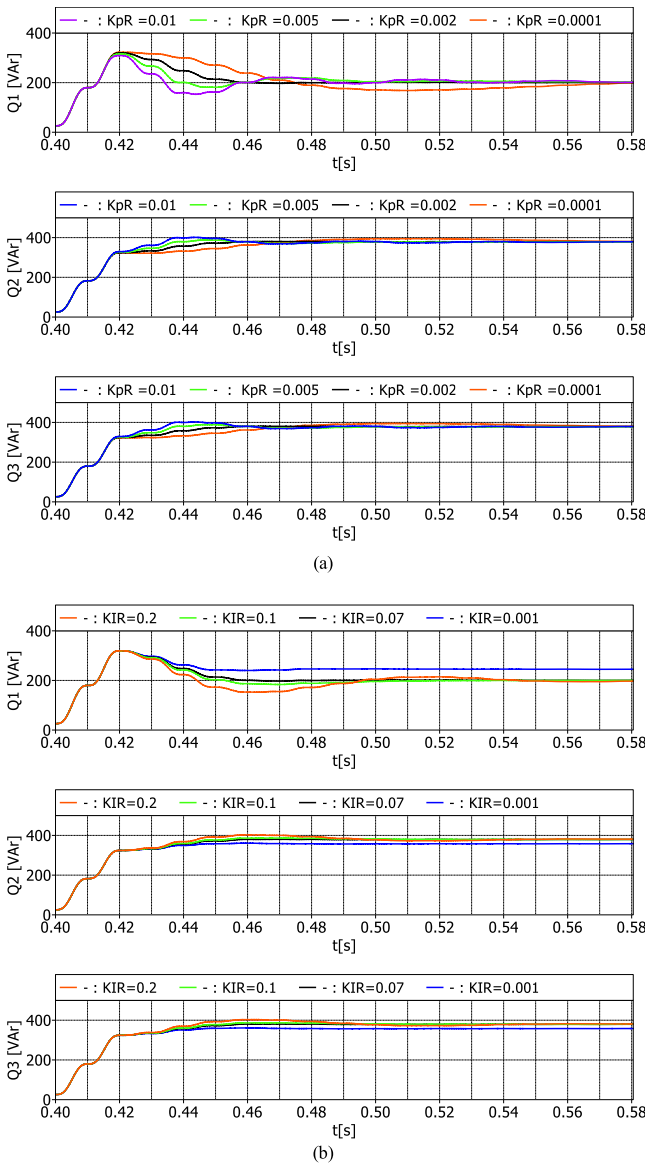

FIGURE 10. Reactive power limitation dynamics (a) varying k_{pR} maintaining k_{IR} constant and (b) varying k_{IR} maintaining k_{pR} constant.

TABLE 3. Settling Times for Different Values of K_{pR}

k_{pR}	0.0001	0.002	0.005	0.01
$t_s[ms]$	170	60	90	130

TABLE 4. Settling Times for Different Values of k_{IR}

k_{IR}	0.001	0.07	0.1	0.2
$t_s[ms]$	∞	60	110	140

change in load of 1 kVAr is introduced with inverter one having its reactive power limited to 0.2 kVAr. The proportional constant k_{pR} is varied while the intergral constant k_{IR} is kept constant at its optimum value. Fig. 10(a) shows the reactive power variations of the three inverters during the transitory process and Table 3 shows the settling times. The optimum value of k_{pR} was found to be 0.002. k_{IR} is then varried, while k_{pR} is kept constant at its optimum value. Fig. 10(b) shows the system reponse and Table 4 shows the settling times, where the minimum settling time was found to be 60 ms at $k_{IR} = 0.07$.

E. INVERTER SYNCHRONIZATION TO THE MG

Before connecting the inverter to the MG, it is necessary to ensure that the phase and voltage magnitude at the output terminal of the inverter are closely matched with those of the MG. This provides a seamless connection with minimal transients. It is important to note that this presynchronization in GFM inverters is done only for the initial connection of

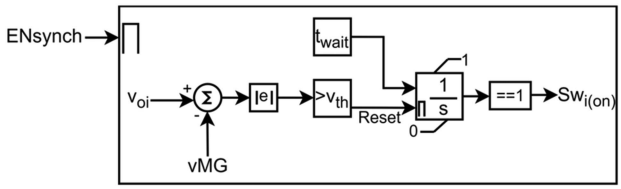

FIGURE 11. Control of Sw1 relay switching after synchronization.

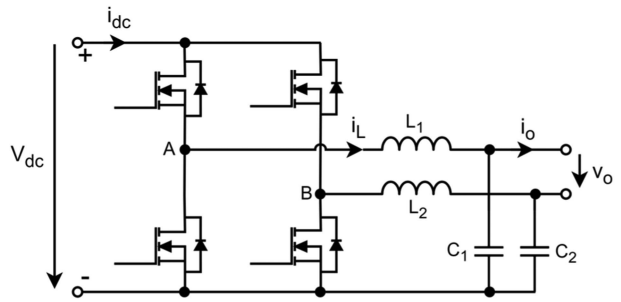

FIGURE 12. Differential single-phase inverter.

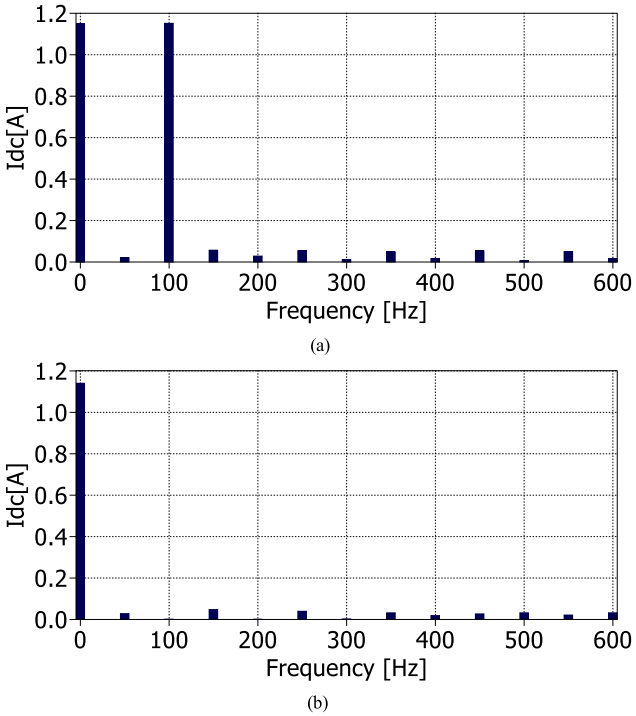

FIGURE 13. FFT of dc-link current: (a) without APD and (b) with APD.

the inverter to the MG. Once the breaker is activated, this synchronization loop is disabled, and the inverter continues to operate governed by the self-synchronizing VOC. In this article, a presynchronization circuit was developed according to [20], represented by the following equation:

$$i_{\text{sync}} = \frac{v_{\text{MG}} - v_{oi}}{k_v R_s} - \frac{v_o}{k_v R_{sh}} \tag{11}$$

where v_{oi} and v_{MG} are the local voltage of the ith synchronizing inverter and the MG voltage, respectively.

The synchronization is based on adding a series virtual resistance R_s and a virtual shunt resistor R_{sh}. The values of these virtual resistances are chosen according to the speed and the accuracy of synchronization. Therefore, after the presynchronization circuit is enabled by EN_{synch}, the added virtual circuit will create a synchronization current [defined by (11)], which is added to the VOC capacitor current. In this way, the VOC reference voltage and phase angle are modified to match those of the MG, thus ensuring synchronization. Before the physical connection to the MG (i.e., closing the relay Sw_1) is executed, a synchronization verification check is done as shown in Fig. 11. After the local voltage matches within a certain threshold v_{th}, with the MG voltage for a certain time t_{wait}, the relay Sw_1 is closed.

F. ACTIVE POWER DECOUPLING

As already mentioned, APD removes the low-frequency oscillations (particularly the second order) from the dc-link current. This is typically achieved by redirecting the oscillating power component to an auxiliary circuit containing film type capacitors. In this article, the single-phase inverter shown in Fig. 12 is implemented to achieve this function. A detailed analysis of this topology is provided in [42]. The main advantage is that it achieves APD without adding additional semiconductor devices and associated components (e.g., drivers and heatsinks), but only the two film capacitors (C_1, C_2). Furthermore, no additional sensors are required beyond those used for controlling the conventional inverter [47]. With the APD function, the size of the capacitance required for the dc-link is reduced, which enables the implementation of an all-film inverter.

The APD is activated by the decoupling controller represented in Fig. 3, which implements the following transfer function:

$$G_d(s) = \frac{v_{\text{comp}}}{V_{dc}} = \sum_{h=2,4,6} \frac{2k_{jD}(h\omega)s}{s^2 + (h\omega)^2} \tag{12}$$

where h and k_{jD} are the harmonic order and the gain of the controller, respectively. More details on the design of this controller are provided in [39].

The APD controller amplifies the second, fourth, and sixth order harmonics present in the dc-link voltage, and its output is added to the modulating voltage as a common mode signal to generate the pulses for the inverter. Because the compensation voltage includes even harmonics, the modulation signal is not centered to half, as in the conventional case, so a signal centering block is added to avoid asymmetrical saturation of the duty cycles by shifting the duty cycles to have equal upper and lower reserves [39]. By this way, the low-frequency power oscillation in the dc-link will be processed by the decoupling capacitors C_1 and C_2. Fig. 13 shows the FFT analysis of the dc-link current with and without APD. It is evident that

TABLE 5. System Parameters

Symbol	Quantity	Value
S	Output apparent power	1 kVA
V_o	Rated output voltage	230 V
f	Rated output frequency	50 Hz
f_s	Switching frequency	40 kHz
V_{dc}	DC-link voltage	450 V
C_{d1}, C_{d2}	Decoupling capacitors	60 μF
L_1, L_2	Filter inductances	280 μH
L_g	Grid side inductance	2.5 mH
VOC parameters		
k_v, k_i	Voltage, current scaling factors	241.5, 0.218
α, σ	Voltage regulation parameters	4.06 A/V^3, 6.09 Ω^{-1}
L, C	Virtual inductance, virtual capacitance	56.3 μH, 0.18 F
Secondary control parameters		
k_{If}, k_{IV}	Voltage, frequency integrator constants	0.002, 0.05
k_{IP}, k_{IQ}	Active, reactive power integrator constants	3, 0.002
Power limitation controller parameters		
k_{pA}	Active power proportional constant	0.001
k_{IA}	Active power integrator constant	0.5
k_{pR}	Reactive power proportional constant	0.0001
k_{IR}	Reactive power integrator constant	0.05

enabling the APD eliminates the low-frequency (i.e., 100 Hz) current component.

III. SIMULATION RESULTS

To demonstrate the performance of the proposed control strategy, a simulation model consisting of three parallel connected inverters, as depicted in Fig. 2, was developed. The controller was implemented in discrete form and the whole controller subsystem was triggered at the PWM sampling period to replicate the operation of a real-time control. The simulations were performed using specialized power electronics software. The parameters of the model are synthesized in Table 5. The simulation results cover various cases of interest to validate the proposed MG operation, as discussed below.

A. PRIMARY CONTROL

In this case, the response of the primary control is tested when the MG is powered by all three inverters. Fig. 14 shows the output currents, active powers, load voltage, and dc-link voltage in the case of a linear resistive load. At $t = 0.4$ and 0.6 s, the second and third inverters are added to the MG following a synchronization procedure discussed further. The dc-link voltage includes the transitory regime at the moment of connecting a new inverter.

A similar analysis is done for a nonlinear load, and Fig. 15 shows the output currents, active powers, load voltage and dc-link voltage. A 1-kVA nonlinear load (bridge rectifier with *RC* load) was used. At $t = 0.4$ and 0.6 s, the second and third inverters are added to the MG. Despite the current absorbed by the nonlinear load being highly distorted the output voltage is maintained quasisinusoidal ($\text{THD}_V = 1.66\%$). The distortion of the output voltage is due to the odd harmonics introduced by the nonlinear load. In both cases, connecting the inverters

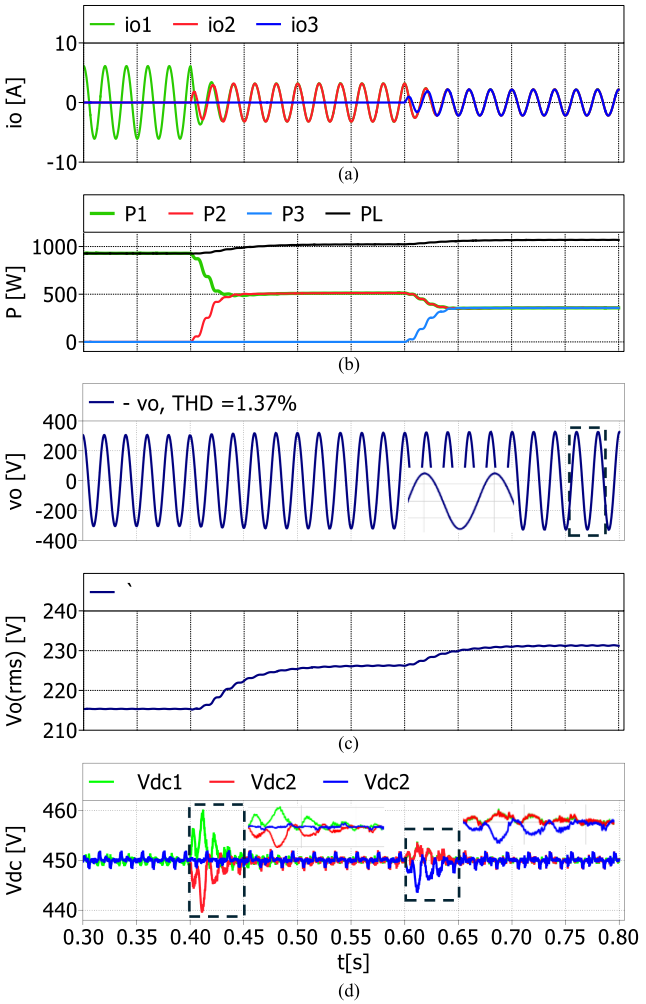

FIGURE 14. Connection of three parallel inverters with linear load: (a) output currents; (b) output active powers; (c) load voltage(v_o, v_{rms}); and (d) dc-link voltages.

does not disturb the MG, while being able to share the powers equally (no limitation is enforced).

B. SECONDARY CONTROL

The ability of the proposed secondary controller to restore the frequency and voltage is analyzed in this section and the results are presented in Fig. 16. The secondary control was tested under two scenarios, one involving a step change in load active power and the other a step change in load reactive power.

In the first case shown in Fig. 16(a), a 1-kW active load is switched ON at $t = 3$ s and OFF at $t = 6$ s. In both scenarios, the secondary control restores the voltage within 2 s. The response of the secondary control to restore the frequency was illustrated through switching ON and OFF a capacitive reactive load ($Q_L = 500$ VAr) at $t = 20$ s and $t = 30$ s, respectively. Fig. 16(b) shows that, within 8 s, the secondary controller restores the frequency to its nominal value. Both voltage and frequency restoration processes follow the designing conditions discussed in Section II-C.

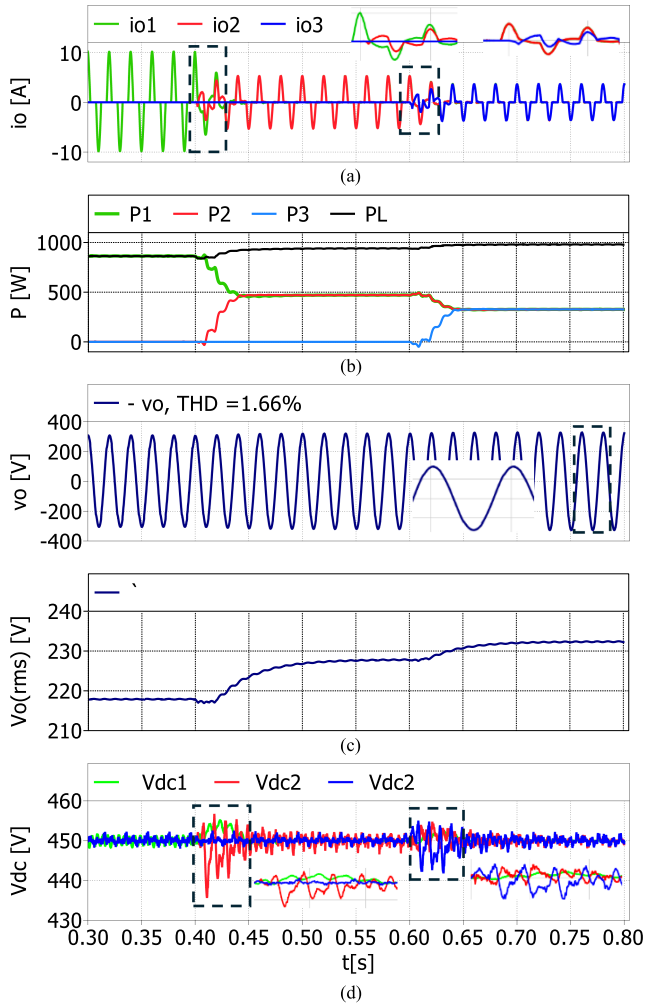

FIGURE 15. Connection of three parallel inverters with nonlinear load: (a) output currents; (b) output active powers; (c) load voltage(v_o, v_{rms}); and (d) dc-link voltages.

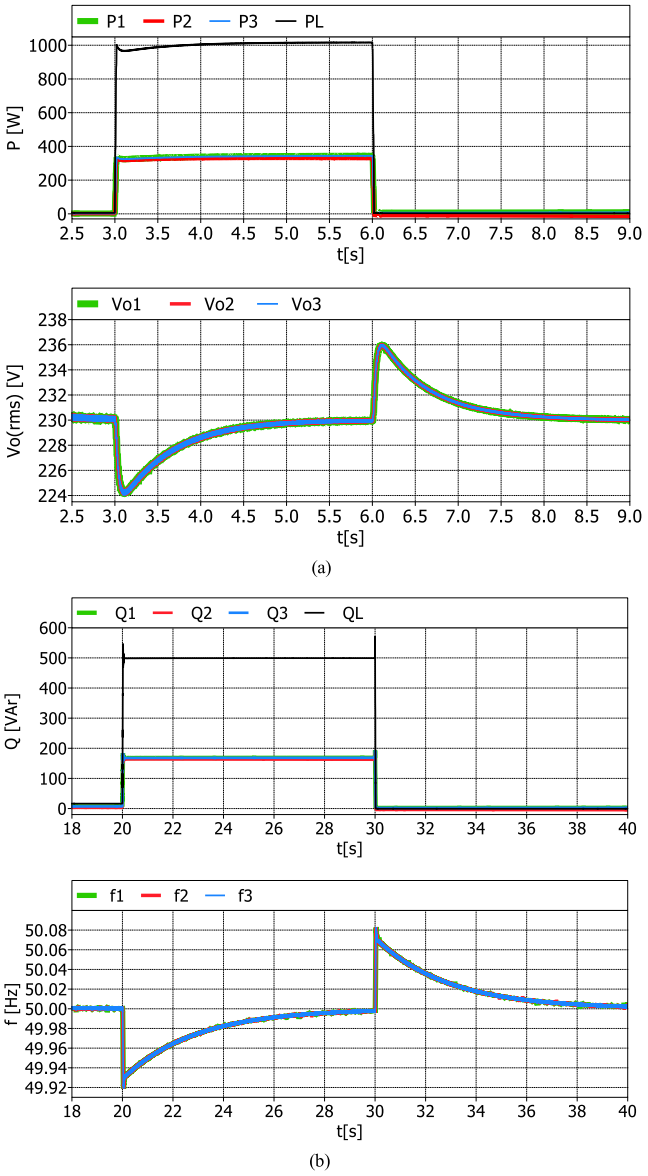

FIGURE 16. Secondary control with the proposed control: (a) step change in active power and (b) step change in reactive power.

C. POWER LIMITATION

The operation of the active power limitation controller is demonstrated in Fig. 17. Two cases were considered to demonstrate the operation of the active power limitation controller. In the first case shown in Fig. 17(a), a 1 kW increase in load active power is introduced at $t = 3$ s and switched OFF at $t = 6$ s. Inverter 1 is considered to have a power limit $P_{\max} = 0.2$ kW. As the power being drawn exceeds $P_{\max}$ for inverter 1, its output power is limited to 0.2 kW. The remaining inverters that operate under their capacity limits supply the extra power to balance the load consumption. In the second scenario shown in Fig. 17(b), the inverters have no power limitation when a step increase in active load is introduced at $t = 3$ s. Therefore, all the inverters share the load power equally. At $t = 6$ s, the active power limit ($P_{\max}$) for inverter 1 is set to 0.2 kW. While inverter 1 reduces its power to 0.2 kW, the other inverters, which have not yet reached their capacity, increase their output power to balance the load consumption. Also, as shown in Fig. 17, the secondary control properly restores the voltage under power limitation in both scenarios presented. Similar implementation was performed to demonstrate the operation of the reactive power limitation controller, and the results are presented in Fig. 18.

In practice, reactive power limitation is enforced when the inverter reaches its capacity due to active power injection. Another case is for optimizing power flow within the MG. To demonstrate the effectiveness of this method, the active powers are maintained constant and vary only the limits of the reactive powers. In the first scenario shown in Fig. 18(a), a step increase in capacitive reactive load (0.5 kVAr) is introduced at $t = 20$ s with inverter 1 having its $Q_{\max}$ set to 0.1 kVAr. Inverter 1 limits its reactive power and the remaining power is supplied by the other inverters with more capacity. At $t = 30$ s, the reactive load is switched OFF. In the second scenario shown in Fig. 18(b), initially, the inverters

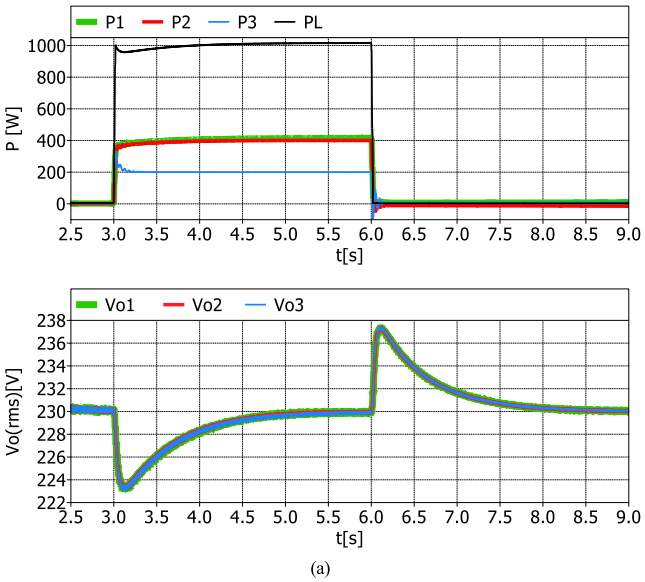

FIGURE 17. Active power limitation: (a) inverter 1 limited during start up and (b) inverters sharing equal power initially, then reduce pmax during operation.

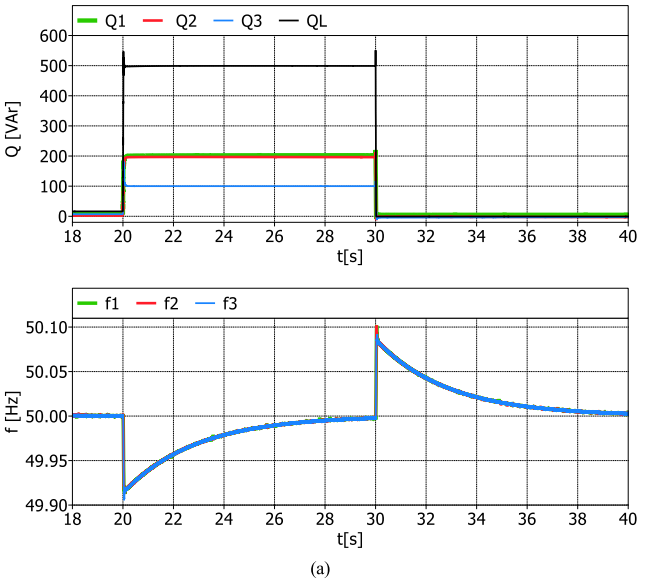

FIGURE 18. Reactive power limitation: (a) inverter 1 limited during start up and (b) inverters sharing equal power initially, then reduce qmax during operation.

share the reactive power equally and $Q_{\max}$ for inverter 1 is set to 0.1 kVAr during operation at $t = 30$ s. The secondary control also restores frequency within 8 s under reactive power limitation.

D. SYNCHRONIZATION

Fig. 19 shows the MG voltage at PCC and the output voltage of one of the inverters before and after synchronization. Before synchronization is enabled, the magnitudes and phase shift of the two voltages are different, as shown in Fig. 19(a). After enabling synchronization (ENsynch = 1) at $t = 0.5$ s, the inverter output voltage quickly aligns to the MG voltage at the PCC. Once the difference between the two voltages is within a certain tolerance (according to the algorithm in Fig. 11), and after the settling time (t_{wait}) has elapsed, the inverter connects to the MG. Fig. 19(b) illustrates the synchronization process described, where inverters 1 and 2 are already connected to the MG, while inverter 3 undergoes synchronization.

IV. EXPERIMENTAL VALIDATION

To validate the simulation results, an experimental setup was built as shown in Fig. 20, according to the MG structure presented in Fig. 2, with the MG setup consisting of two inverters. Due to their implementation, one with IGBT and the other with silicon carbide (SiC) transistors, the switching frequencies of the inverters are 20 and 40 kHz, respectively. A

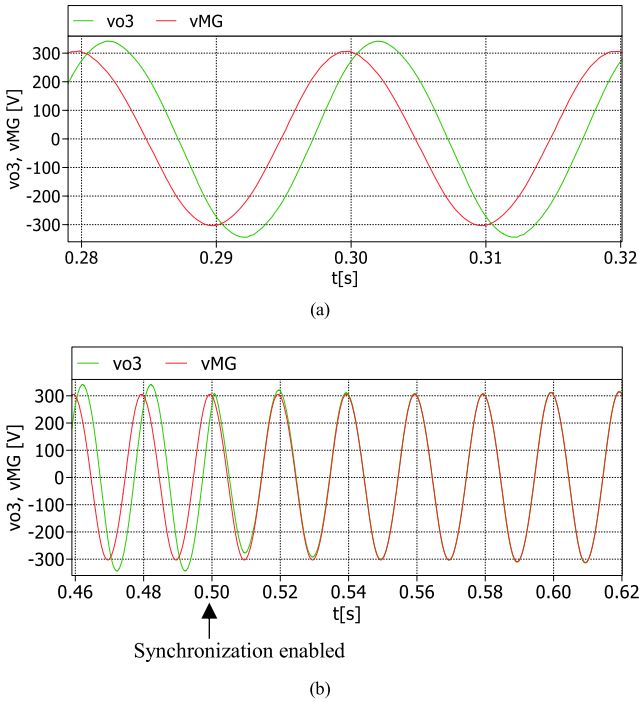

FIGURE 19. Synchronization process: (a) before synchronization and (b) synchronization enabled.

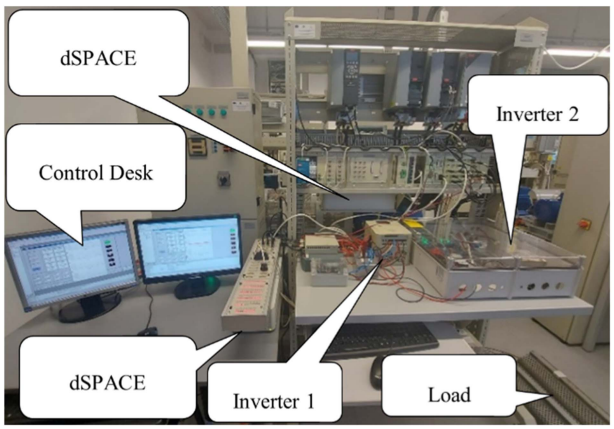

FIGURE 20. Experimental setup of the proposed MG.

switching frequency of 40 kHz was chosen based on the efficiency analysis presented in [48] for this type of SiC inverter. For the IGBT inverter, the switching frequency (20 kHz) was selected based on the implementation of a similar inverter in [39]. The other parameters are shown in Table 5. Each inverter was controlled by a separate dSPACE DS1103 controller, and the waveforms were acquired through ControlDesk software. The communication between the inverters for the secondary controller implementation was achieved through a CAN communication protocol. Two separate dc power supplies were used as primary sources for the two inverters. The inverters control is discretized in Simulink before being programed into dSPACE. The sampling frequency was chosen to be equal to

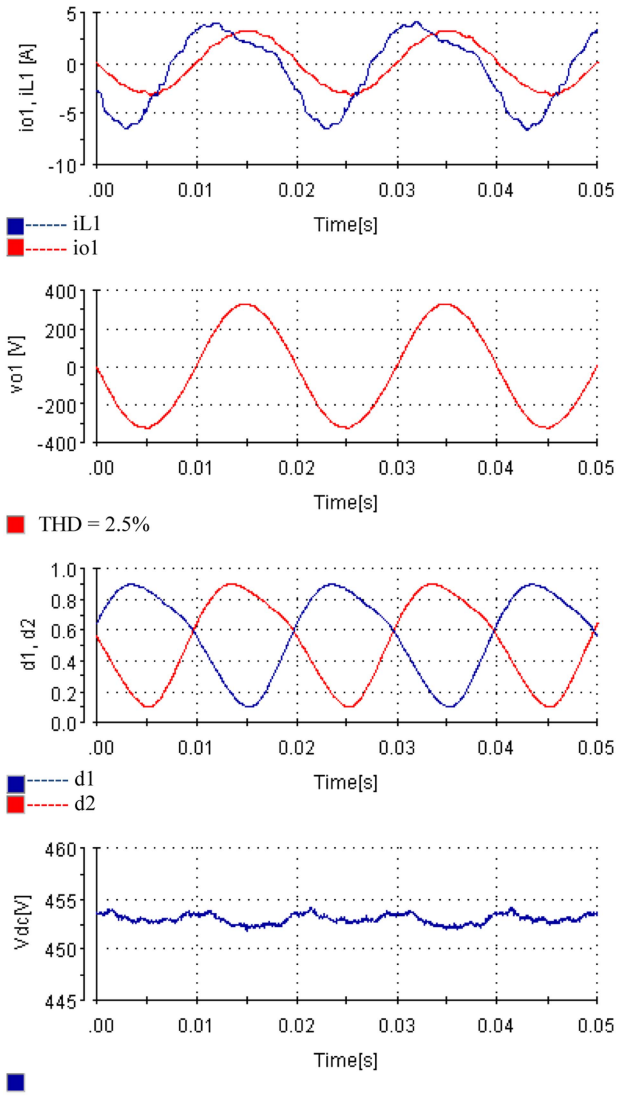

FIGURE 21. Inverter steady-state waveforms: output and inductor current, output voltage, duty cycles, and dc-link voltage.

the switching frequency of the inverters. The voltages and currents were measured using Hall effect transducers (LV25NP for voltages and LA55P for currents) and the resulting signals are provided to the processor's ADCs. The numerical resolution of the analog signals is 16-bit, while the processor uses floating-point number representation. The PWM generator has a time step of 100 ns and uses 16 bit registers, thereby its resolution depends on the switching frequency, i.e., 8.9 bit for the IGBT inverter and 7.9 bit for the SiC inverter.

The analysis presented below synthesizes different case scenarios to experimentally validate the operation of the proposed system.

A. PRIMARY CONTROL

In this case, the main signals of one of the two inverters forming the MG are provided. Fig. 21 shows the currents [filter current (i_{L1}) and inverter output current (i_{o1})], output

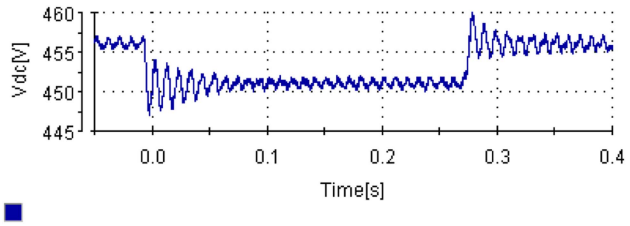

FIGURE 22. DC-link voltage when there is step change in load.

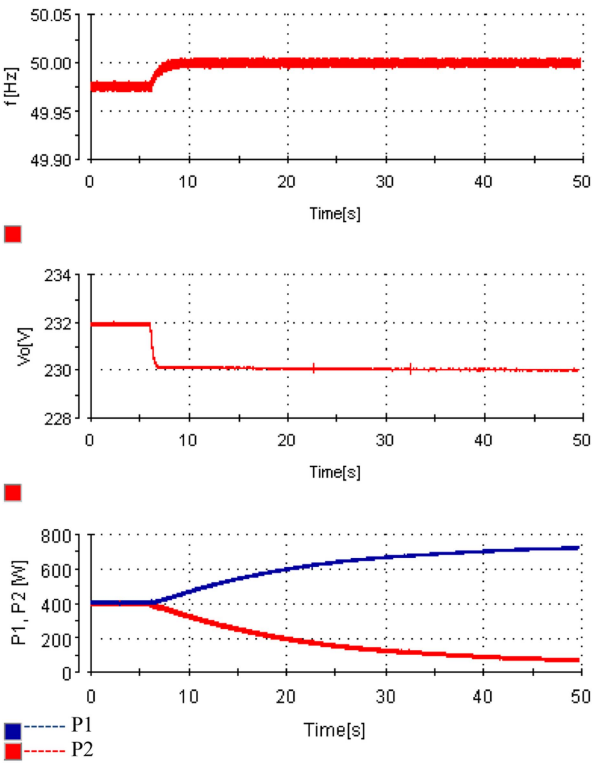

FIGURE 23. Secondary control with local integrators.

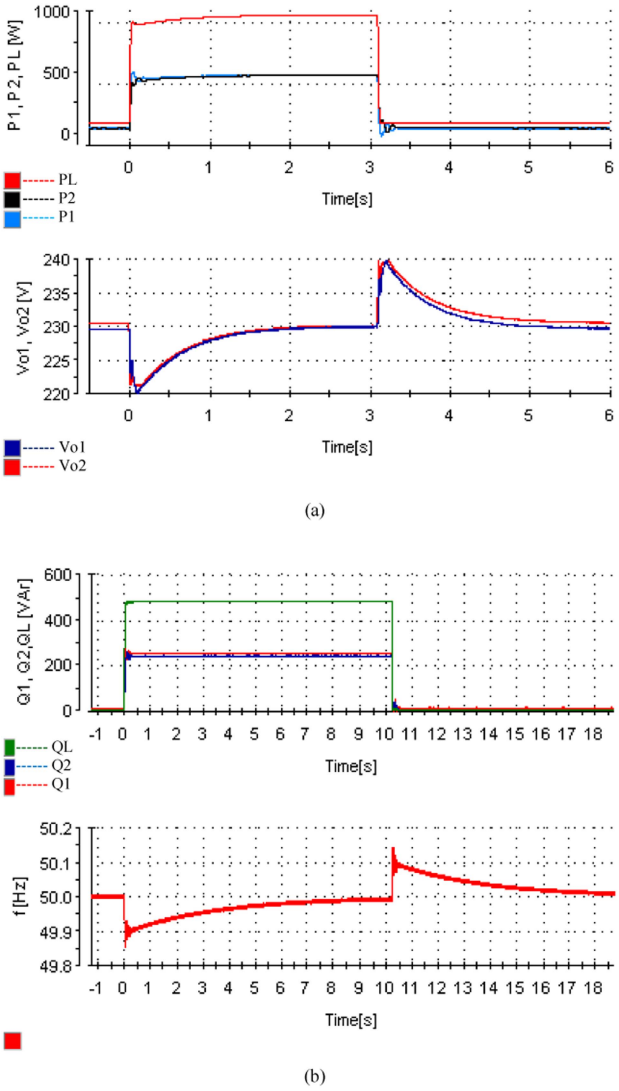

FIGURE 24. Secondary control with the proposed control: (a) step change in active power and (b) step change in reactive power.

voltage, duty cycles, and dc-link voltage with a linear resistive load. It is important to note that i_{L1} and duty cycles (d_1, d_2) are not purely sinusoidal due to the common mode compensation voltage containing even harmonics added to the modulating signals to achieve APD. However, the output voltage is not affected as it is a differential component. The THD of the output voltage is 2.5%. Another source of voltage distortion is the inherent third harmonic introduced by the VOC. The effect of APD on the dc-link voltage is shown in Fig. 21, where the low-frequency oscillations have been significantly eliminated. Fig. 22 shows the dc-link voltage including transitory regime when a step change of 1-kW active load is introduced at $t = 0$ s and $t = 2.8$ s. It can be seen that the oscillation stabilizes within approximately 50 ms.

B. SECONDARY CONTROL

To demonstrate the effect of clock drift on the performance of the secondary controller, a decentralized secondary control was implemented with only local integrators and no communication between the inverters. The results are shown in Fig. 23. The secondary control was enabled at $t = 6$ s. Despite the controller being able to regulate the frequency and voltage to their nominal values, it can be observed that the active powers continue to diverge as time progresses because of clock drift, resulting in an unstable equilibrium operating condition.

With the implementation of the proposed secondary control method, where each inverter exchanges information about the active and reactive powers, the challenges introduced by the clock drift are curtailed. Furthermore, the proposed secondary control maintains power sharing, ensuring proportional power contribution from each inverter and preventing excessive strain on any unit.

To evaluate the accuracy of the active and reactive power sharing of each unit, the power sharing error of the ith unit

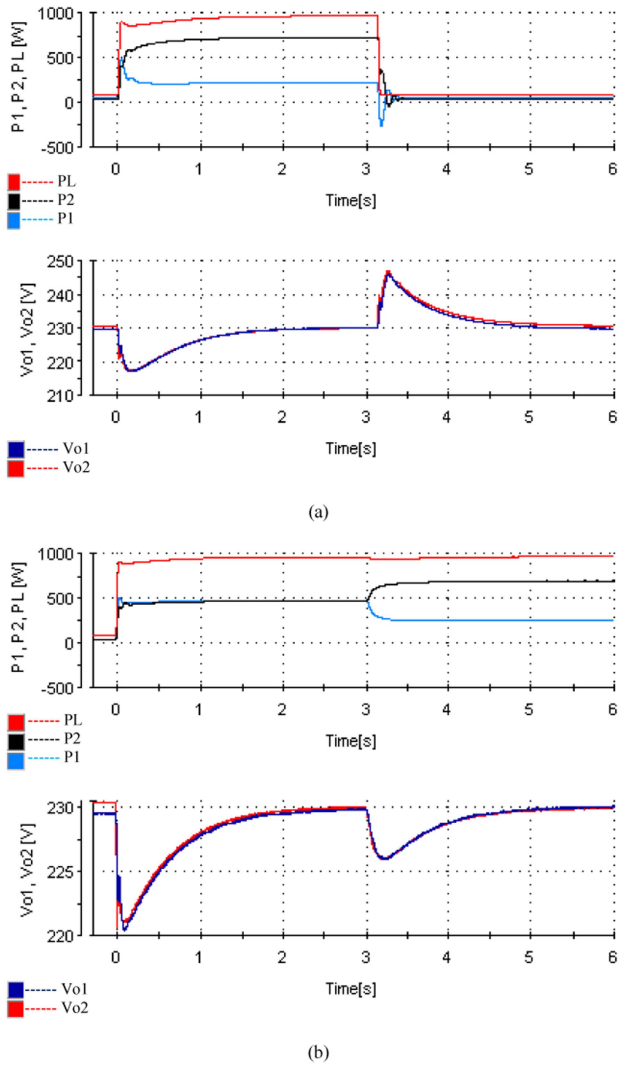

FIGURE 25. Active power limitation: (a) inverter 1 limited during start up and (b) inverters sharing equal power initially, then reduce pmax during operation.

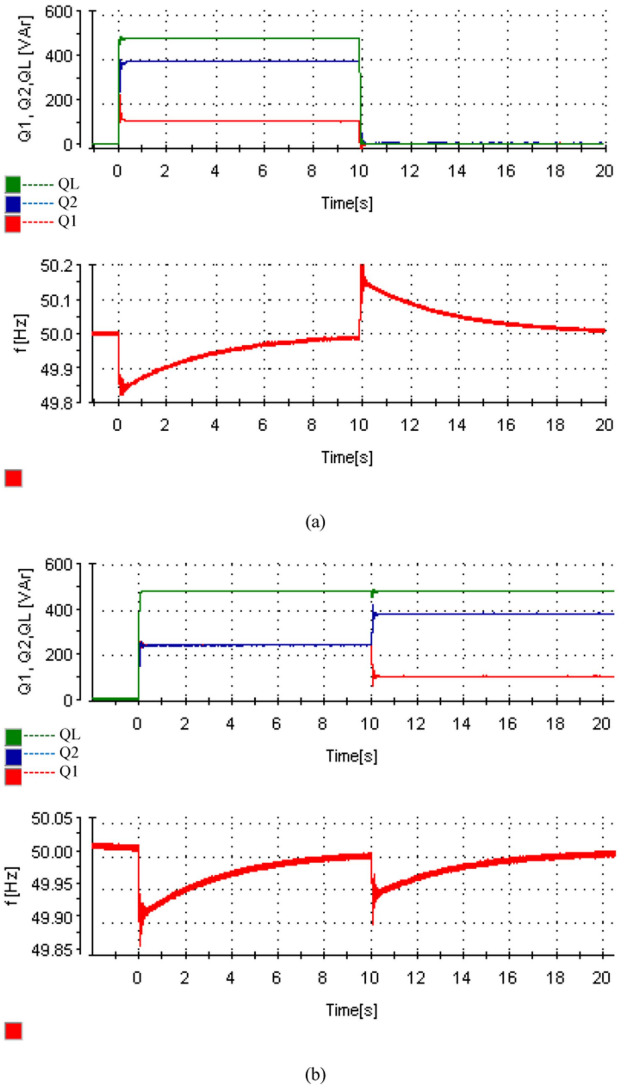

FIGURE 26. Reactive power limitation: (a) inverter 1 limited during start up and (b) inverters sharing equal power initially, then reduce qmax during operation.

can be defined as follows:

$$P_{\text{err}(i)\ \%} = \left| \frac{P_{(i,\text{ref})} - P_i}{P_{(i,\text{ref})}} \right| .100 \tag{13}$$

$$Q_{\text{err}(i)\ \%} = \left| \frac{Q_{(i,\text{ref})} - Q_i}{Q_{(i,\text{ref})}} \right| .100 \tag{14}$$

where $P_{(i,\text{ref}}$ and $Q_{(i,\text{ref})}$ are the reference active and reactive power, respectively. P_i and Q_i are the actual inverter output powers of the ith unit.

As shown in Fig. 23, $P_{\text{err}\ (i)\ \%}$ and $Q_{\text{err}\ (i)\ \%}$ diverges with time. Fig. 24(a) shows the performance of the proposed secondary control when there is a step change in load active power (P_L). At $t = 0$ s, a 1-kW load is introduced, and at $t = 3.1$ s the load is turned OFF. In both cases, the secondary control restores the voltage within around 2 s, while maintaining power sharing. As shown in the figure, the power sharing error of inverter 1 and 2, $P_{\text{err}\ (1,2)\ \%} \cong 0\%$. A similar scenario was also performed to test the response of the secondary control to a step change in reactive power (Q_L). Fig. 24(b) shows the reactive powers supplied by each inverter, the load power and the frequency. In both cases of turning ON and OFF the reactive load, the frequency was restored within around 8 s. In this particular case, $Q_{\text{err}\ (1)\ \%} \cong 4\%$ and $Q_{\text{err}\ (2)\ \%} \cong 0.7\%$. As can be seen, the experimental results closely align with the simulations.

C. POWER LIMITATION

As already described, the power limitation controller can limit the output power of the converter depending on its operating conditions. To experimentally validate the operation of the active power limitation controller, two scenarios were considered. In the first case presented in Fig. 25(a), a step increase

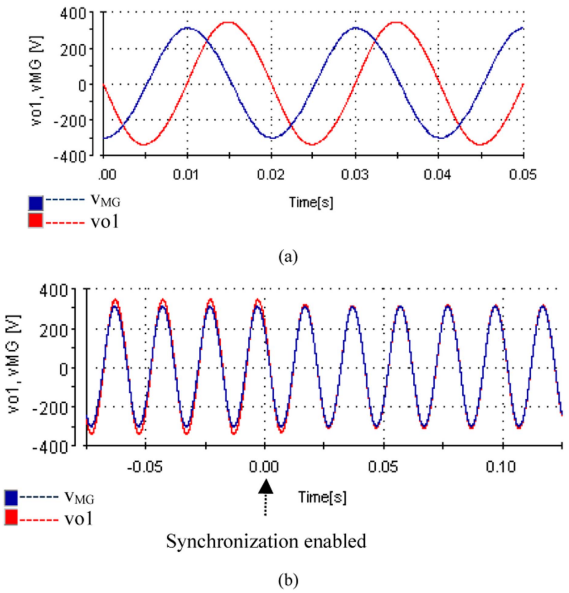

FIGURE 27. Synchronization process: (a) before synchronization and (b) synchronization enabled.

of active power (1 kW) is introduced at $t = 0$ s, with inverter 1 having its active power limited to 0.25 kW and inverter 2 having no power limitation. The power supplied by inverter 2 is constrained only by its capacity (1 kVA). During a step increase in load, inverter 1 limits its output active power to 0.25 kW, and the other inverter that has not yet reached its limit increases its output power to balance the load consumption. At $t = 3.1$ s, the load is switched OFF. As shown in Fig. 25(a), the secondary control also restores voltage under active power limitation constraints. In the second case shown in Fig. 25(b), the inverters are initially turned ON with equal power sharing (no power limitation enforced). At $t = 3$ s, $P_{\max}$ for inverter 1 is reduced to 0.25 kW. As shown, inverter 1 limits its output active power to $P_{\max}$, while the remaining power is provided by inverter 2. Additionally, the results prove that the secondary control restores the voltages during power limitation.

Similar scenarios are tested for the reactive power limitation controller and the results are presented in Fig. 26. In case 1, a step increase in reactive load is introduced at $t = 0$ s, with inverter 1 having its reactive power limited to 0.1 kVAr. As shown in Fig. 26(a), inverter 1 limits its reactive power and inverter 2 supplies the remaining load power. In case 2 shown in Fig. 26(b), $Q_{\max}$ for inverter 1 is changed to 0.1 kVAr at $t = 10$ s. Its output power is reduced to 0.1 kVAr demonstrating the ability of power limitation to control the power dispatched by the inverter. The results also demonstrate that the secondary control restores the frequency within 8 s.

D. SYNCHRONIZATION

Before synchronization, deviations in both the magnitude and the phase are observed between the MG voltage at the PCC and the inverter output voltage. As the frequencies of these two signals are different initially, this implies that the rate at which their phases are changing is different. So the phase difference is a function of time. Fig. 27(a) shows the phase difference at a particular instant before synchronization. Once synchronization is enabled, the two signals are matched both in terms of amplitude and phase, ensuring a seamless connection of the inverter to the MG. Fig. 27(b) shows the synchronization process. At $t = 0$ s, synchronization is enabled, and the inverter connects to the MG after the two signals match within the acceptable tolerance for a certain time (t_{wait}).

VI. CONCLUSION

The need to effectively control and manage diverse distributed energy resources necessitates more research on MG control strategies. To manage the intermittent nature of renewable energy sources and the constraints posed by primary sources, this article presented a power limitation controller for VOC-based inverters to dispatch power according to the operating conditions of the primary source. The controller successfully limited both the active and reactive power supplied by the inverters, which is essential for optimizing primary source's capacity utilization and preventing inverter overload. Furthermore, this article developed a secondary controller integrated with the VOC, designed to be robust against the effects of clock drifts in digital controllers. To this end, a decentralized secondary controller using a distributed averaging approach was implemented. The proposed controller restored the frequency and voltage to its nominal value while maintaining power sharing. Finally, an APD control was implemented in the VOC-based inverters to eliminate the low-frequency components in the dc-link. Various case scenarios were considered through simulations and experiments to analyze the performance of the proposed controllers, and the main results are summarized as follows.

1) The parallel operation of inverters with the proposed VOC control and APD ensured proper regulation of the load voltage; experimental measurements showed a voltage THD of 2.5%, which is well within the typical limit of 8% set by IEEE 519-2022 power quality standards.
2) The power limitation controller effectively limited both the active and the reactive power of each converter in less than 100 ms, without affecting the MG control performance.
3) The developed secondary controller effectively regulated the frequency in 8 s and voltage in 2 s as validated by both the simulation and the experiments; experimental implementation showed the effectiveness of the proposed method to maintain accurate power sharing despite the presence of challenges such as clock drifts inherent in digital controllers. The active power sharing error for both inverters (P_{err} (1,2) %) was nearly zero, while for reactive power sharing the errors were negligible (<5%). Furthermore, by using distributed

averaging, the conflict between voltage regulation and active power sharing was minimized.

4) For connecting the inverter to the MG, a presynchronization circuit was developed ensuring seamless connection of each inverter.

Future article will focus on expanding the control system to three phase inverters for higher power applications, and on the compatibility analysis with other classical GFM techniques such as droop control and VSM.

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