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SURVEY

Differential Single-Phase Inverters With Active Power Decoupling: A Survey

RONALD MUSONA AND IOAN SERBAN, (Member, IEEE)
Department of Electrical Engineering and Applied Physics, Transilvania University of Brasov, 500036 Brasov, Romania
Corresponding author: Ioan Serban (ioan.serban@unitbv.ro)

ABSTRACT This paper provides an overview of differential single-phase inverter topologies with active power decoupling (APD) and their main control techniques. Owing to the advantage of achieving APD without additional semiconductor devices, thus boosting inverter reliability at a minimum cost, these topologies have gained increasing interest, especially for small-scale photovoltaic applications. Therefore, in this study, we consider it essential to synthesize the main differential single-phase inverters, their operating principles, and provide a unified mathematical description for each topology. The study identified and analyzed three main structures: buck, boost, buck–boost, and derived topologies. First, a comparative analysis, including a hardware assessment in terms of the DC-link voltage requirements, voltage and current stresses on the switches, and losses, shows the performance of various inverter topologies under different operating parameters (e.g., input voltage and decoupling capacitance). Second, this paper discusses the main control strategies applied to this class of inverters to achieve both primary control (autonomous or grid-connected operation) and APD functions, while highlighting the development of control algorithms that are less dependent on parameter variations and more robust to external disturbances. Finally, the need for further research on reliability improvement in single-phase differential inverters, particularly in the context of emerging technologies, such as high-speed switches (e.g., wide-bandgap semiconductors) and advanced control techniques, is emphasized.

INDEX TERMS Single-phase differential inverter, active power decoupling, wide-bandgap semiconductors, photovoltaics.

NOMENCLATURE

APD	Active power decoupling
CM	Common mode
DBB	Differential buck-boost
DBO	Differential boost
DBU	Differential buck
DBU-SC	Differential buck with split capacitor
DM	Differential mode
DSCHB	DC split capacitor for H-bridge
GaN	Gallium nitride
HB	Half Bridge
HPF	High pass filter
PCC	Point of common coupling
PFC	Power factor correction
PI	Proportional Integral
PR	Proportional Resonant
PV	Photovoltaic
RES	Renewable energy sources
RS-DSCHB	Reduced switch DC split capacitor for H-bridge.
SiC	Silicon carbide
WBG	Wide bandgap

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I. INTRODUCTION

As an important segment of power electronics, single-phase inverters are widely used today in a variety of small-scale applications (i.e. kW range), such as renewable energy sources (RES), on-board chargers of electric vehicles, home appliances, or uninterruptible power supplies [1], [2], [3]. Consequently, there has been increased research interest in

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both hardware topologies and control solutions for single-phase inverters, with a focus on improving reliability, reducing costs, increasing efficiency, and enhancing power density [4], [5], [6]. The adoption of wide-bandgap (WBG) semiconductors, such as silicon carbide (SiC) and gallium nitride (GaN), which have been proven to outperform traditional silicon-based transistors (at least in small-scale applications) by higher voltage and temperature ratings, faster switching speeds, and lower losses [7], [8], [9], [10], represents an important path towards achieving the aforementioned goals. The size and weight of magnetic components, such as inductors, are reduced when the switches are operated at high switching speeds, thereby lowering the cost and enhancing the power density [11]. However, the switching losses are a function of the switching frequency; hence, the optimum switching frequency is a compromise between the power loss and the reduction in the cost and size of the magnetic components.

To achieve high efficiency and good system performance of GaN converters at high switching frequencies (in the MHz region), soft switching has been suggested as opposed to hard switching, which has been shown to achieve high efficiency at switching frequencies in the kHz region [4], [12], [13]. In this regard, triangular current modulation was proposed in [14], [15], and [16] to achieve soft switching, in [4], a 1kW GaN based single phase inverter was implemented with 98% efficiency and 120W/in^3 power density. A 99% peak efficiency and 220W/in^3 power density were also demonstrated in [17] for a 1.2kW GaN-based MHz totem-pole PFC rectifier with triangular current modulation.

Another major challenge in single-phase inverters is the processing of the inherent second-order power oscillation component, which must be prevented from being transferred to a DC source [18], [19], [20]. The processing of low-frequency ripples requires high energy storage. Conventionally, passive decoupling techniques that utilize large DC-link electrolytic capacitors have been used. However, because of the relatively short lifetime of electrolytic capacitors, also highly dependent on temperature [21], [22], [23], other solutions have been investigated in literature which are commonly referred to as active power decoupling (APD) techniques [24], [25], [26], [27], [28]. The main idea behind APD solutions is to direct the inherent power oscillation to a more reliable short-term energy storage element such as a thin-film capacitor, which is referred to as a decoupling capacitor. It is important to note that the energy storage element can be capacitive or inductive. However, despite the reliability of inductors, capacitors are commonly used owing to their lower power losses and costs [29], [30]. The decoupling capacitors can be placed on the DC or AC sides of the inverter [27]. In [24], [26], and [31], a review was conducted on active power decoupling topologies, and a generic topology derivation method was provided. Two different techniques are commonly used in active power decoupling methods to transfer pulsating power to a buffering

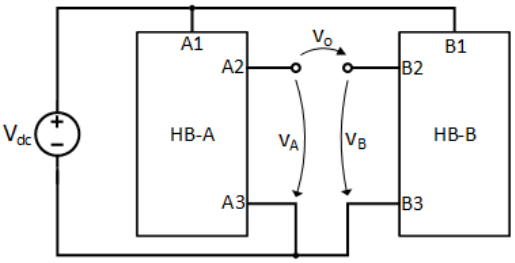

FIGURE 1. Generic structure of single-phase differential inverters.

component. The first involves adding active switches to the converter circuit, such as a third leg [32], [33], [34], and the second does not add any additional active elements. The use of extra semiconductor devices to achieve power decoupling affects the power density, cost, and efficiency of the converter [35], [36]. Therefore, differential inverters are a suitable option for achieving active power decoupling without the need for additional semiconductor components. Because of their small component count, they offer a cost-effective solution for handling the second-order ripple component in single-phase inverters. Unlike the conventional H-bridge inverter, which suffers from leakage current [37], [38], [39], the differential inverter mitigates the effects of leakage current, as analyzed in [40], making it suitable for photovoltaic (PV) applications. The two decoupling capacitors on the AC side in the differential inverters provide a conducting path to high-frequency common-mode currents, preventing the leakage current from flowing through the parasitic capacitance. Leakage current reduces converter efficiency and raises safety concerns [41], [42], [43]; therefore, it must be controlled below the level that complies with standard requirements.

Although several survey studies on APD solutions are available in literature, no comprehensive investigation of the differential inverter class has been conducted. Therefore, this study seeks to fill this gap by providing the main features and a comparative performance analysis in terms of the DC-link voltage requirements, losses, and stresses on the inverter components.

The general structure of a voltage source differential single-phase inverter is illustrated in Fig. 1. It consists of two half-bridge (HB) converters (A and B) that operate in either differential mode or common mode. The differential mode transfers power from the input port to the output port, and the common mode is used to achieve power decoupling. Each half-bridge is a DC-DC converter that can be configured as a buck, boost, or buck-boost topology. Starting from these basic topologies, different inverter topologies can be identified, namely differential buck (DBU), differential boost (DBO), differential buck-boost (DBB), and differential buck inverters with split capacitors on the AC side (DBU-SC). In addition, other topologies to achieve active power decoupling, such as an H-bridge with a DC split capacitor (DSCHB) and its reduced switch inverter (RS-DSCHB), are also considered.

TABLE 1. A timeline of the active power decoupling topologies for differential inverters.

Topology	Publication year										Decoupling controller	Load type
	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022		
DBU	[44]										Analytical reference generation	Linear
			[18]								Multi resonant	Linear
			[45]								Multi resonant	Grid
			[46]								HPF + PR	Linear
			[35]								HPF + PR	Grid
			[47]								Multi resonant	Grid/ Linear
			[48]								HPF + PR	Linear
				[49]							Multi resonant	Grid
						[50]					Multi resonant	Linear / nonlinear
								[51]			Multi resonant	Linear
									[52]		Analytical reference generation	Grid
									[53]		Multi resonant	Linear / nonlinear
										[20]	Multi resonant	Linear
										[54]	Multi resonant	Linear
										[55]	Multi resonant	Linear
										[56]	Multi resonant	Linear
DBO			[48]								HPF + PR	Linear
			[57]								Bandpass filters	Grid
			[58]								Rule based controller	Grid
				[59]							Analytical reference generation	Linear
						[50]					Multi resonant	Linear / nonlinear
										[60]	Multi resonant	Linear / nonlinear
DBB			[48]								HPF + PR	Linear
					[61]						Analytical reference generation	Linear
						[50]					Multi resonant	Linear /nonlinear
						[62]					Analytical reference generation	Linear
						[63]					HPF + Even frequency repetitive controller	Nonlinear
DBU-SC										[64]	Analytical reference generation	Linear
DSCHB		[65]									PR	Grid
				[19]							Multi resonant	Grid
							[66]				Total sliding mode controller	Grid
									[67]		Analytical reference generation	Linear
RS-DSCHB		[29]									PR	Grid
			[68]								Multi resonant	Grid / Linear

A timeline of the analyzed differential inverter topologies with active power decoupling, with the main references that provided a new approach that led to the development of the considered topology, is shown in Table 1.

The vertical axis represents the topology as defined in this study, whereas the horizontal axis represents the year in which the reference was published, as well as the types of decoupling controllers and loads (linear/nonlinear, autonomous operation, or grid-connected). As shown in Table 1, most of the contributions were made to the DBU inverter, which was found to be the most practical, as also revealed in this study. As detailed in Section IV, the developed decoupling controllers are mainly based on structures that amplify the voltages or currents at frequencies associated with the pulsating power.

The main emphasis in the controller design is the development of autonomous control algorithms that are less sensitive to parameter variations and more robust to external disturbances. Control methods for active power decoupling can be broadly categorized into four types [69]: power balance-based control, harmonic suppression-based control, virtual impedance-based control, and volt-second/charge balance-based control.

In addition to the second harmonic component generated by the instantaneous power pulsating at twice the fundamental frequency, additional harmonics are introduced when the inverter interfaces with nonlinear loads, such as rectifiers and appliances, using switched-mode power supply conversion technologies [70], [71], [72]. Nonlinear loads, drawing current in pulses, introduce odd-order harmonics. When these

harmonics flow to the DC side, they become additional even harmonics, which degrade the inverter performance.

Although more attention has been given to APD with linear loads, additional research still needs to be conducted for nonlinear loads. The impact of nonlinear loads on differential inverters was studied in [50], [53], [73], and [74], and a harmonic compensation strategy was introduced to compensate for the harmonics. Another application of single-phase inverters is the integration of renewable energy into the grids. Power grids are nonideal and hence present low-frequency harmonics at the point of common coupling (PCC) [75], [76], [77].

To achieve precise power decoupling, a neural filter was utilized in [66] to adaptively extract ripple voltage for use in decoupling control. The impact of the capacitance mismatch caused by age-related variations in storage capacitance in differential single inverters requires further research. When there is a capacitance mismatch, additional first- and third-order current harmonics are introduced on the DC side, which, if not mitigated, cause the second- and fourth-order current harmonics to flow to the grid. This requires the controller to compensate for the additional harmonics. The effects of these harmonics can be a problem for grid-connected inverters that are required to meet grid standards such as IEEE 1547, which limits the second to tenth even harmonics of the current to 1% [78]. In [79], a control scheme was proposed to mitigate the effects of capacitor mismatches in a differential buck inverter.

The remainder of this paper is structured as follows. In Section II, we describe the analyzed APD differential inverter. In Section III, we present an analysis of the voltage and current stresses of the switches, as well as the corresponding losses, along with experimental validation. Section IV provides an overview of the main control solutions adopted for APD differential inverters and the damping in single-phase inverters. In Section V, we discuss some open research challenges for single-phase inverters with APD. Finally, Section VI presents the main conclusions of this study.

II. DIFFERENTIAL SINGLE-PHASE INVERTER TOPOLOGIES

As shown in Fig. 1, differential single-phase inverters can be viewed as two synchronous half-bridges (HB-A and HB-B) that are supplied by a common DC source. A synchronous half-bridge inverter has two switches that operate in a complementary manner and a filter inductor connected to the midpoint. A filter capacitor is also added to the output to provide low-pass filtering together with the inductor. HB-A and HB-B are connected in parallel to the same DC input source, and each half-bridge is modulated such that the differential output voltage across the two half-bridges is sinusoidal. This generic topology is configurable, and depending on the component arrangement, it can be configured to implement one of three fundamental topologies: buck, boost, or buck-boost. Fig. 2 to Fig. 4 show the schematics of the DBU inverter, DBO, and DBB, respectively. The midpoint between the two decoupling capacitors C_1 and C_2 is connected to the negative terminal of the DC source. A similar operation is obtained if the common

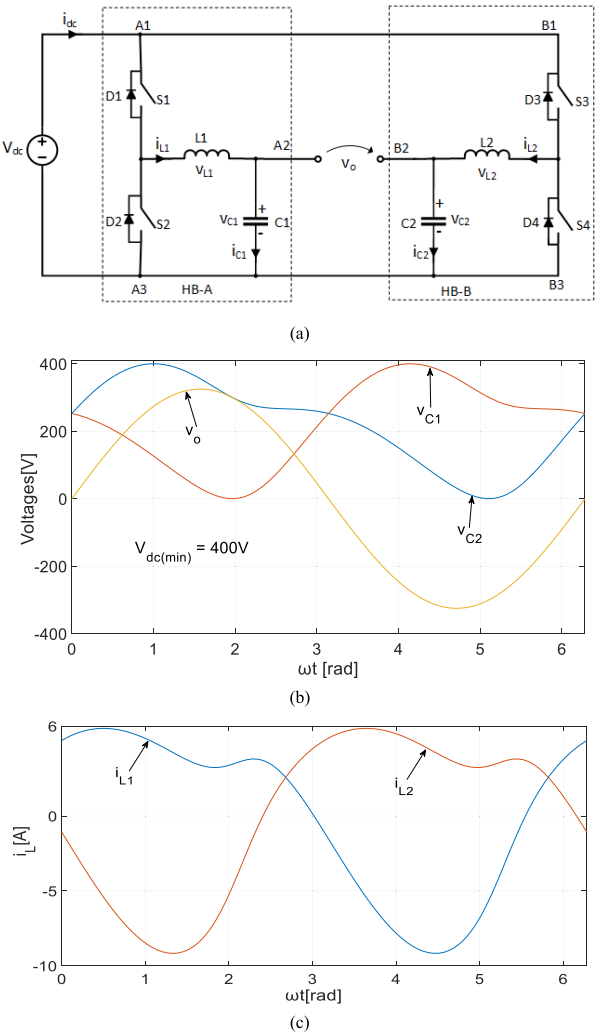

FIGURE 2. Differential buck single-phase inverter: (a) Topology; (b)Voltage waveforms of v_{C1}, v_{C2}, v_O; (c) Current waveforms of i_{L1} and i_{L2}.

point of the decoupling capacitors is connected to the positive rail. The two terminals, A2 and B2, on the AC side are then connected differentially across the load or grid. Other topologies can be generated from these fundamental topologies, as in [64], in which the initial decoupling capacitors on the AC side of the differential buck inverter are divided into two symmetrical forms. Fig. 5 shows the derived differential buck inverter with an AC side-split capacitor (DBU-SC). In [80], the midpoint of the two decoupling capacitors was connected to the midpoint of the split DC-link capacitor. Thus, the utilization of decoupling capacitors is improved.

The output voltage of the differential single-phase inverter, as shown in Fig. 1, is generated as a differential component between the two output ports of the two half-bridges (A2, B2). Without power decoupling, the two HB output voltages are controlled to follow the references shown in (1) with the same magnitude and frequency but 180° out of phase.

$$\begin{cases} v_A = V_d + 0.5V_m sin(\omega t) \\ v_B = V_d - 0.5V_m sin(\omega t) \end{cases} \tag{1}$$

TABLE 2. Inverter main parameters.

Parameter	Value
Output voltage (rms) and frequency	230V, 50Hz
Rated output active power	1 kW
Decoupling capacitance (C_1, C_2)	60 µF

where V_d, V_m and ω are the DC voltage offset, maximum amplitude of the output voltage, and angular frequency, respectively.

The differential mode (DM) component, which is the output voltage, is given by (2).

$$v_o = v_A - v_B = V_m sin(\omega t) \tag{2}$$

A. ACTIVE POWER DECOUPLING IN DIFFERENTIAL BUCK INVERTER

Suppose that the inverter topology DBU shown in Fig. 2(a) supplies a linear load with a sinusoidal output voltage, given by (2), the instantaneous output power p_o is given by (3).

$$p_o = \frac{V_m I_m}{2}[cos\phi - cos(2\omega t + \phi)] \tag{3}$$

where I_m is the amplitude of the output current and ϕ is the phase angle between v_o and the output current i_o.

The inherent second-order power component in (3) must be decoupled to prevent it from being transferred to the DC source. As noted in the introduction, instead of using a large aluminum capacitor on the DC side, power decoupling in the analyzed topologies is achieved by diverting the power pulsation to a more reliable thin-film capacitor of lower capacity.

Neglecting the voltage drop on the output inductors, the power absorbed by the decoupling capacitors must be equal to the power of the oscillating component. This leads to the formulation of the following first-order differential equation (4),

$$C_1 v_{c1}\frac{dv_{c1}}{dt} + C_2 v_{c2}\frac{dv_{c2}}{dt} = \frac{V_m I_m}{2} cos(2\omega t + \phi) \tag{4}$$

For symmetrical loading of the inverter, it was assumed that ($C_1 = C_2 = C_d$). Knowing the differential output voltage ($v_{C1} - v_{C2}$) given in (2) and solving (4) and (2), the two output voltages result in (5), where S is the apparent power, V_o is the RMS of the output voltage, and K_0 is an initialization parameter, as explained below.

Based on the operating constraint of a half-bridge, the voltages across the two decoupling capacitors must be positive, as shown in (6), as shown at the bottom of the next page. Moreover, the part under the square root of (5), as shown at the bottom of the next page must also be positive. These two constraints can be fulfilled by parameter K_0, which can be calculated as in (7), as shown at the bottom of the next page.

If the controller can reshape v_{C1} and v_{C2} to follow (5), active power decoupling can be achieved. However, this method is parameter-dependent; hence, precise power decoupling may not be achieved if parameters such as capacitance, change, or disturbances exist in the output current. For the main parameters provided in Table 2 and considering $\phi = 0$ (which will be considered the same in the following analysis), Fig. 2(b) shows the obtained voltage waveforms v_{C1} and v_{C2} across the decoupling capacitors and the differential output voltage (v_o) under nominal capacitance at rated power.

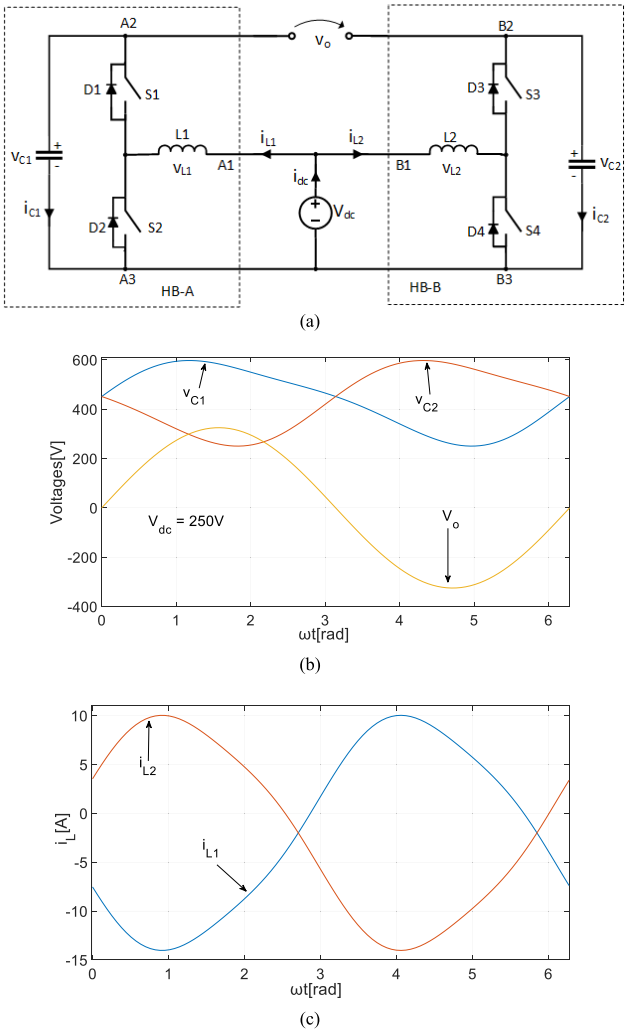

FIGURE 3. Differential boost single-phase inverter: (a) Topology; (b) Voltage waveforms of v_{C1}, v_{C2}, v_O; (c) Current waveforms of i_{L1} and i_{L2}.

The results show that the maximum voltage of the decoupling capacitance is approximately 1.23 times the maximum value of the output voltage. Hence, the minimum DC input voltage required in this case is greater than that of the conventional H-bridge. Fig. 2(c) shows the inverter output current waveforms (i_{L1} and i_{L2}).

B. ACTIVE POWER DECOUPLING IN DIFFERENTIAL BOOST INVERTER

The general topology of a DBO inverter is shown in Fig. 3(a). The general equation for v_{C1} and v_{C2} remains the same as that of the DBU topology, as shown in (5), and only K_0 is changed to satisfy the new constraint (8) introduced for the differential

boost inverter.

$$v_{c1,2} \geq V_{dc} \quad \forall \in \omega t[0, 2\pi] \tag{8}$$

where V_{dc} denotes the input DC voltage. In this case, K_o is obtained by numerically solving (9).

$$K_0 = \max_{0\leq\omega t\leq 2\pi}\left[4V_{dc}^2 - 4\sqrt{2}V_{dc}V_o sin(\omega t) + 4V_o^2 sin^2(\omega t) - \frac{2S}{\omega C_d}[sin(2\omega t - \phi) + sin(\phi)]\right] \tag{9}$$

The waveforms of the decoupling capacitances v_{C1} and v_{C2}, and the output differential voltage (v_o), are shown in Fig. 3(b). The capacitor voltages are shifted above the DC input voltages. The advantage of this topology is that it can operate with a lower DC input voltage. However, because the voltage across the decoupling capacitors is shifted above the DC input voltage, the decoupling capacitors experience higher voltage stresses. Fig. 3(c) shows the inverter current waveforms.

C. ACTIVE POWER DECOUPLING IN DIFFERENTIAL BUCK-BOOST INVERTER

The basic structure of DBB is shown in Fig. 4(a). It consists of two buck-boost converters (HB-A and HB-B) connected to the same DC input source V_{dc}. The output voltage v_o is the differential voltage across the two decoupling capacitors C_1 and C_2. The DBB can operate in either buck or boost mode depending on the input DC voltage. Similarly, the voltage equations, v_{C1} and v_{C2} remain the same as those of the DBU, as shown in (5). In the buck mode, the value K_0 is given by (7), whereas in the boost mode, it is given by (9). Although this topology has a wider operating range for the DC input voltage, the voltage stress across the inverter leg is the highest (sum of the DC input voltage and the voltage across the decoupling capacitor). Fig. 4(b) and Fig. 4(c) show the waveforms of the decoupling capacitances v_{C1} and v_{C2} for the boost and buck modes, respectively. Fig. 4(d) and Fig. 4(e) show the output current waveforms for the boost and buck modes, respectively. For practical reasons, a DC voltage of 250V was considered for boost mode [50].

D. ACTIVE POWER DECOUPLING IN DIFFERENTIAL BUCK INVERTER WITH SPLIT CAPACITOR ON THE AC SIDE

This topology, shown in Fig. 5(a), is derived from DBU [64]. The decoupling capacitors are split into two symmetrical forms. The filtering loop created by the DC source and capacitors C_1, C_3 or C_2, C_4 provides a conducting path for high-frequency switching ripples, which reduces the requirements of DC-link capacitors. The oscillating component is processed using all four capacitors, as shown in (10), with constraints (2) and (11).

$$C_1 v_{c1}\frac{dv_{c1}}{dt} + C_2 v_{c2}\frac{dv_{c2}}{dt} + C_3 v_{c3}\frac{dv_{c3}}{dt} + C_4 v_{c4}\frac{dv_{c4}}{dt} = 0.5V_m I_m cos(2\omega t + \phi) \tag{10}$$

$$\begin{cases} v_{c1,2,3,4} \geq 0 & \forall\, \omega t \in [0, 2\pi] \\ v_{ci} = V_{dc} - v_{c(i-2)} & \forall\, \omega t \in [0, 2\pi],\ \{i = 3, 4\} \end{cases} \tag{11}$$

Solving differential equation (10) with constraints (2) and (11) yields (12), where K_o is obtained by numerically solving the following expression (13).

The decoupling capacitor waveforms v_{C1}, v_{C2}, v_{C3}, v_{C4} are shown in Fig. 5(b), and Fig. 5(c) shows the inverter current waveforms (12) and (13), as shown at the bottom of page 8.

E. ACTIVE POWER DECOUPLING FOR H-BRIDGE INVERTER WITH DC SPLIT CAPACITOR AND REDUCED SWITCH INVERTER

To provide a balanced analysis, the H-bridge topology with an additional leg for APD, DSCHB [19], and its derived reduced switch, RS-DSCHB [29], as shown in Fig. 6(a) and Fig. 6(b), respectively, were also considered. In Fig. 6(a), an additional synchronous buck leg is added to the H-bridge inverter. The DC-link capacitor is also split into two identical capacitors connected in series. The advantage of these topologies is that no additional capacitors are required for the APD, as the same DC-link capacitors will perform the dual functionalities of maintaining a stiff DC-link bus voltage and performing active power decoupling. The decoupling circuit is a synchronous buck circuit with DC split capacitor. To minimize the number of semiconductors used, a reduced switch topology (Fig. 6(b)) is used, which offers the advantage of reduced cost, similar to differential single-phase inverters. Fig. 6(c) and Fig. 6(d) show the decoupling capacitor voltage waveforms and inverter currents, respectively.

The midpoint of one leg is connected to the midpoint of the split DC-link capacitor through a small filter inductor *L1*. The ripple oscillations are absorbed by the DC-link capacitors through modulation of this phase leg. For RS-DSCHB, the second leg must also be modulated to ensure that the output voltage and current are sinusoidal. The current loading of the two inverter legs is different because the other leg performs an additional role in achieving APD. The general equation (4)

$$v_{c1,2} = \pm\frac{V_m}{2}sin(\omega t) + \frac{1}{2}\sqrt{\frac{2S}{\omega C_d}sin(2\omega t - \phi) - 2V_o^2 sin^2(\omega t) + \frac{2S}{\omega C_d}sin(\phi) + K_0} \tag{5}$$

$$v_{c1,2} \geq 0 \quad \forall\, \omega t \in [0, 2\pi] \tag{6}$$

$$K_0 = \max_{0\leq\omega t\leq 2\pi}\left[4V_o^2 sin^2(\omega t) - \frac{2S}{\omega C_d}[sin(2\omega t - \phi) + sin(\phi)\right] \tag{7}$$

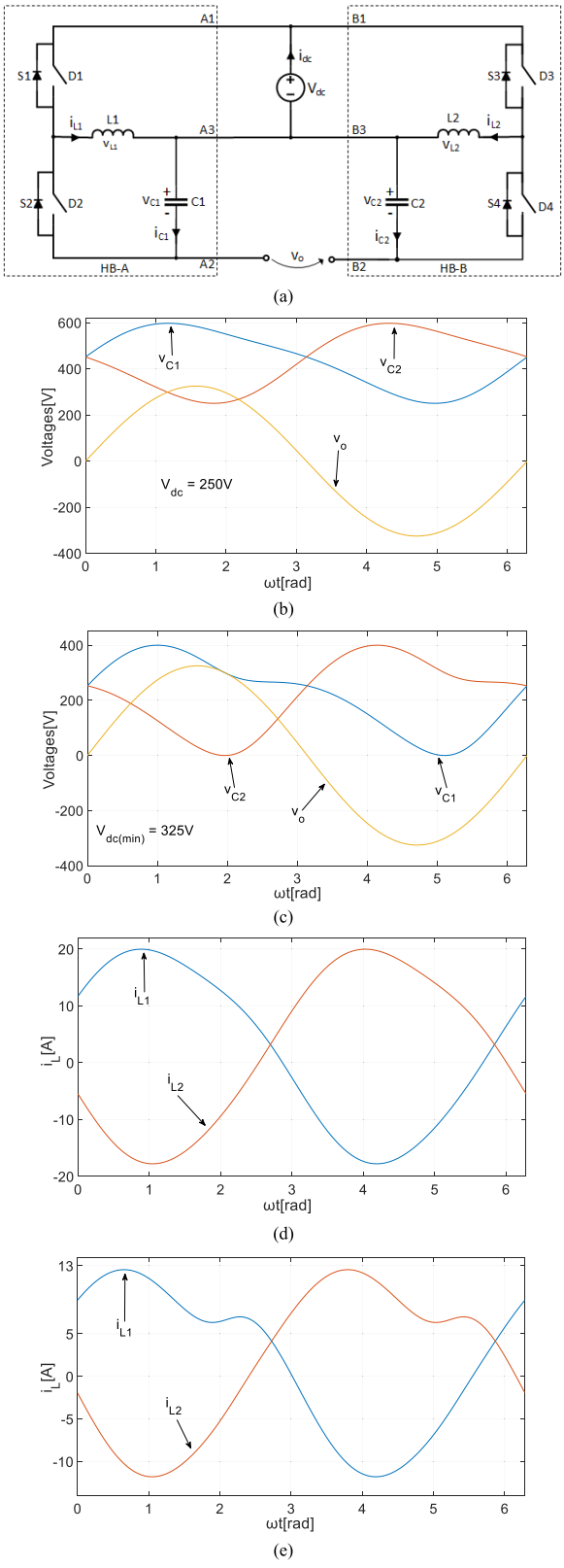

FIGURE 4. Differential buck-boost single-phase inverter: (a) Topology; (b) Voltage waveforms of v_{C1}, v_{C2}, v_O in boost mode; (c) Voltage waveforms of v_{C1}, v_{C2}, v_O in buck mode; (d) Current waveforms of i_{L1} and i_{L2} in boost mode; (e) Current waveforms of i_{L1} and i_{L2} in buck mode.

holds for these two topologies with the following constraints:

$$\begin{cases} v_{c1,2} \geq 0 \quad \forall\, \omega t \in [0, 2\pi] \\ v_o = V_m sin(\omega t) \\ v_{c2} = V_{dc} - v_{c1} \end{cases} \tag{14}$$

Solving equation (4) with the above-mentioned constraints yields equation (15), where K_o is given by optimization of the function (16).

$$v_{c1} = \frac{V_{dc}}{2} + \frac{1}{2}\sqrt{V_{dc}^2 + \frac{2S}{\omega C_d}[sin(2\omega t - \phi)] + sin(\phi) - K_o} \tag{15}$$

$$K_0 = \min_{0 \leq \omega t \leq 2\pi}\left[V_{dc}^2 + \frac{S}{\omega C_d}[sin(2\omega t - \phi)] + sin(\phi)\right] \tag{16}$$

The voltage waveforms of v_{C1} and v_{C2} across the decoupling capacitors for the minimum V_{dc} under nominal capacitance and rated power are shown in Fig. 6(c), whereas Fig. 6(d) shows the inverter current waveforms.

III. VOLTAGE STRESS, CURRENT STRESS, AND LOSSES OF APD DIFFERENTIAL INVERTERS

Adding a compensation voltage to achieve active power decoupling results in an increase in the voltage stress on the decoupling capacitors and switches, or an increase in the DC-link voltage requirement. The voltage stress on the switch is considered as the voltage across the inverter leg. From the considerations in Table 3, a voltage stress analysis is performed, where V_{cmax} is the maximum voltage on the decoupling capacitors.

The plot of the minimum voltage stresses on the switches as a function of the decoupling capacitance for the buck and boost topologies is shown in Fig. 7(a) and Fig. 7(b), respectively. As can be seen, the overall voltage stress on the inverter leg decreased as the capacitance increased. This is because for the same capacitor energy, the voltage of the capacitor is inversely proportional to the square root of the capacitance. Fig. 7(a) shows that the differential buck topology has the lowest switch voltage stress. This makes it possible to use switches with comparatively low voltage ratings, which lowers their price. In addition, having a higher safety margin on the switches is beneficial for improving reliability. Moreover, the low-voltage stress on the switches translates to low switching losses, which improves the inverter efficiency and the requirements of the cooling system. In contrast, DBB (in the buck mode) exhibited the highest voltage stress. Among the boost topologies (Fig. 7(b)), DBO has a low voltage stress on switches compared to DBB (in boost mode). Above 60μF it can be noted in Fig. 7(a) that the switch voltage stress on DSCHB is lower than that on RS-DSCHB to maintain a voltage v_{M2} positive. The switch stresses of the DBB inverter topology are a combination of the DC link

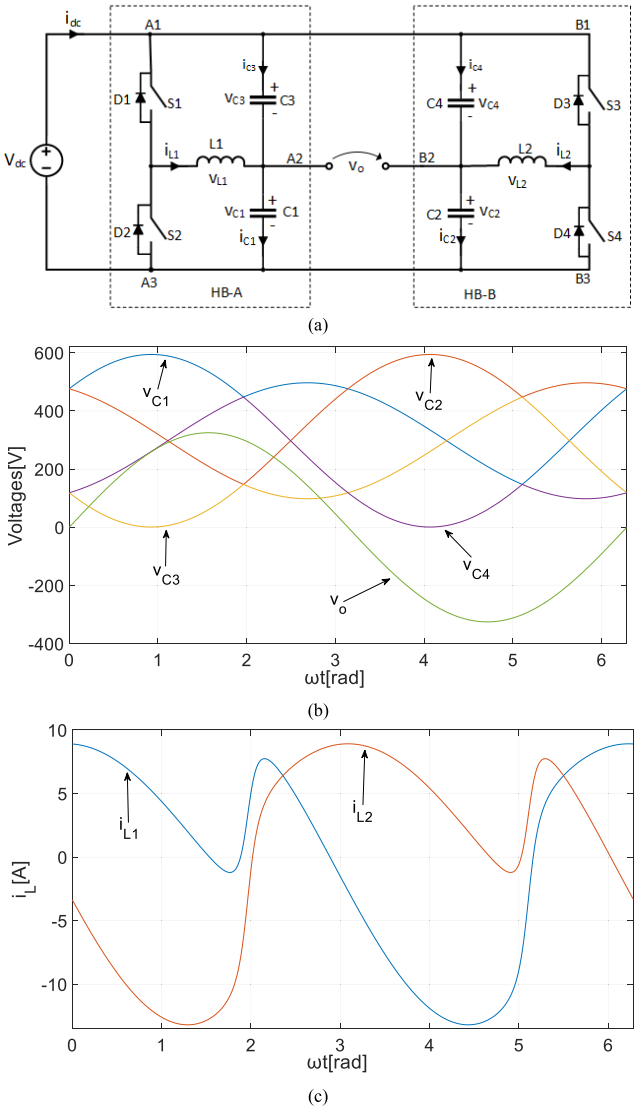

FIGURE 5. Differential buck inverter with split capacitor on the AC side: (a) Topology; (b) Voltage waveforms of v_{C1}, v_{C2}, v_{C3}, v_{C4}, v_O; (c) Current waveforms of i_{L1} and i_{L2}.

voltage and the stress in the decoupling capacitor, which makes it higher than those of the other topologies.

To analyze the inverter current stresses, the RMS current through the filter inductor was considered, and the plots are shown in Fig. 8(a) and Fig. 8(b) for the buck and boost topologies, respectively. As shown, the current stress increases as the decoupling capacitance increases. The inverter current stress is important for determining the losses

TABLE 3. Voltage limits for switches and decoupling capacitors.

Topology	Voltage stress on the switches	Voltage constraints on the decoupling capacitors
DBU	V_{dc}	$0 \le V_{c1,2} \le V_{dc}$
DBO	V_{cmax}	$V_{c1,2} \ge V_{dc}$
DBB	$V_{dc}+V_{cmax}$	$V_{c1,2} \ge 0$
DBU-SC	V_{dc}	$V_{c1,2,3,4} \ge 0$
DSCHB	V_{dc}	$V_{c1,\,c2} \ge 0$
RS-DSCHB	V_{dc}	$V_{c1,\,c2,\,M1,\,M2} \ge 0$

of the switches. Moreover, high current stress implies the need to use filter inductors with a higher saturation current. Therefore, the optimum value of the decoupling capacitance should be a compromise between losses and component size. Among the buck topologies, the differential buck topology also has lower inverter currents, while for boost topologies, the differential boost topology has a lower inverter current.

A. SWITCH UTILISATION

As mentioned previously, the minimum number of switches is the main advantage of the analyzed inverter topologies. However, the increase in voltage and current stress implies that the semiconductors are oversized. Often used to analyze converter performance, switch utilization (SU) indicates the ratio between the output power delivered by the converter and the total active switch stress, defined as [81]:

$$SU[\%] = \frac{V_m I_m}{\sum_{k=1}^{n} V_{sk} I_{sk}} \cdot 100 \tag{17}$$

where: V_m, I_m are the inverter peak output voltage and current; V_{sk}, I_{sk} are the maximum voltage and current of the n switches.

Table 4 shows the SU of the analyzed inverters, considering the operating conditions corresponding to $C_d = 60\mu$F, as discussed previously.

B. LOSSES ANALYSIS

Along with minimum complexity, another important feature that must be considered in the analyzed topologies is efficiency. As previously shown, ensuring power decoupling requires an increase in the voltage and current stress on the transistors, which is expected to lead to increased losses in semiconductors. Therefore, this section analyzes the losses (switching and conduction) of the investigated topologies in comparison with the conventional H-bridge inverter. As single-phase inverters are expected to use wide-bandgap

$$v_{c1,2} = \frac{V_{dc}}{2} \pm \frac{V_m}{2} sin(\omega t) + \frac{1}{2}\sqrt{V_{dc}^2 - 2V_o^2 sin^2(\omega t) + \frac{S}{\omega C_d}[sin(2\omega t - \phi)] + sin(\phi)] - K_o} \tag{12}$$

$$K_0 = \min_{0 \le \omega t \le 2\pi} \left[V_{dc}^2 - 2V_o^2 sin^2(\omega t) + \frac{S}{\omega C_d}[sin(2\omega t - \phi)] + sin(\phi) \right] \tag{13}$$

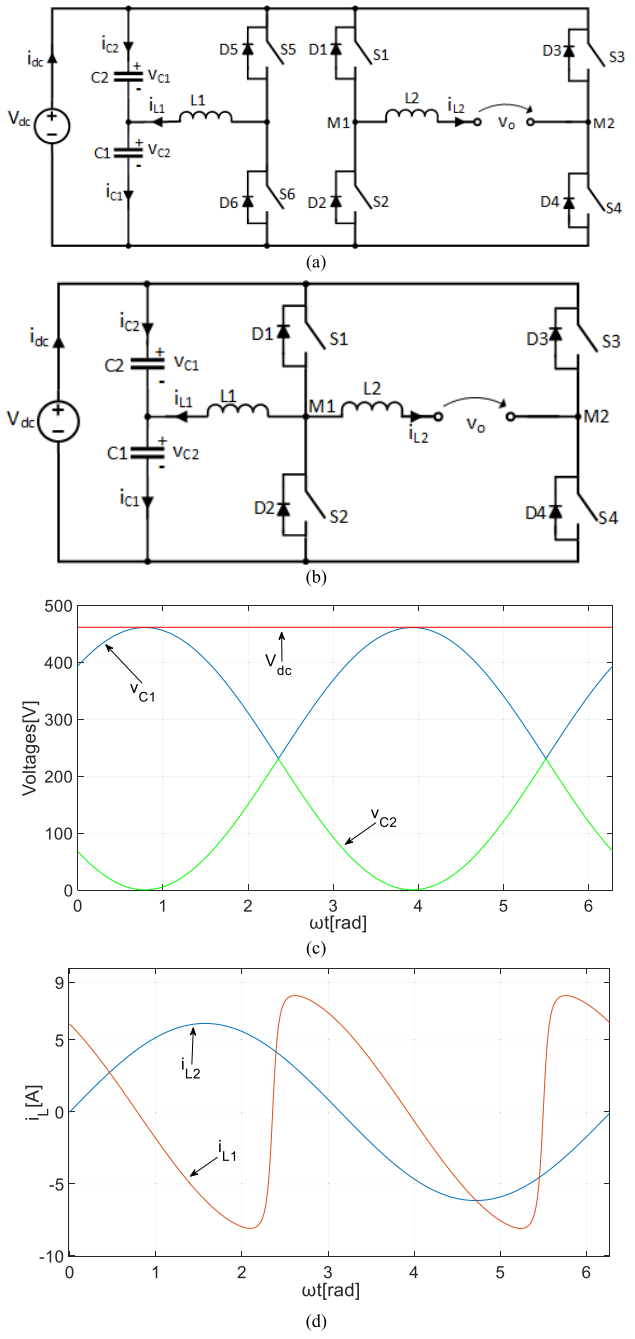

FIGURE 6. H-Bridge inverter with DC-slit capacitor: (a) H-Bride inverter with synchronous buck active power decoupling; (b) Reduced switch topology; (c) Voltage waveforms of vC1, vC2, vC3, vC4; (d) Current waveforms of i_{L1} and i_{L2}.

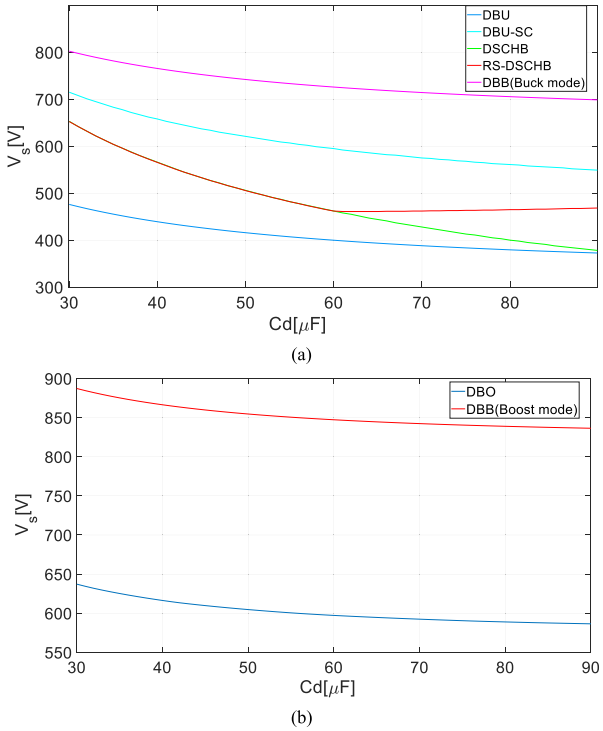

FIGURE 7. Voltage stress: (a) Buck topologies; (b) Boost topologies.

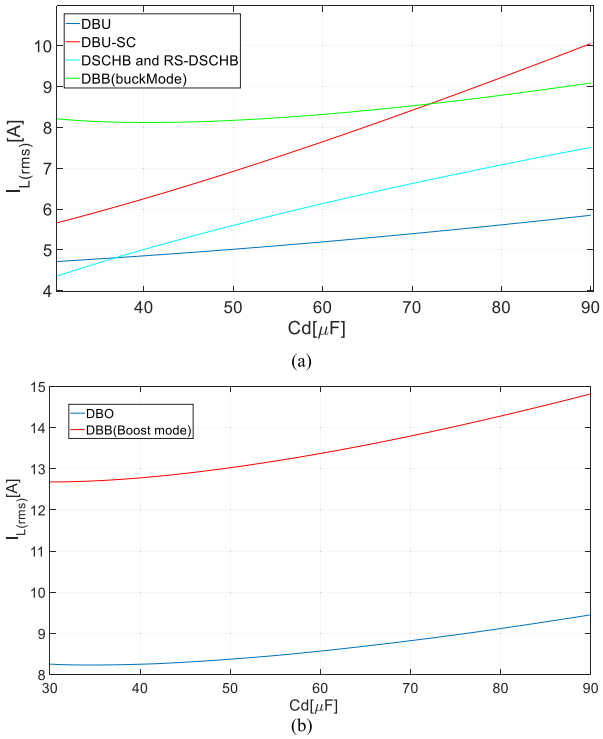

FIGURE 8. Current stress: (a) Buck topologies; (b) Boost topologies.

MOSFETs (SiC and GaN) in the future, this analysis focuses on the unique characteristics of these transistors in terms of both conduction and switching losses. Additionally, for the purpose of simplification and generalization, the conduction and switching losses are analyzed separately and normalized considering as base values the conduction and switching losses of a conventional H-bridge inverter that uses the same MOSFET type and operates under similar conditions. The voltages and currents previously determined for each topology were considered in the calculation of conduction and switching losses. Considering the same capacitance for the decoupling capacitors ($C_d = 60\mu$F), Table 5 presents the

TABLE 4. SU of the analysed inverter topologies.

Topology	SU [%]
Conventional	25.0
DBU	13.6
DBO	6.0
DBB (boost mode)	3.0
DBB (buck mode)	5.5
DBU-SC	6.4
DSCHB	9.8
RS-DSCHB	13.6

TABLE 5. Optimum voltages (DC source and half bridge).

Topology	DC Source (V_{dc}) [p.u.]	Half bridge DC-link voltage [p.u.]
Conventional	1.00	1.00
DBU	1.23	1.23
DBO	0.77	0.77 – 1.84
DBB (buck mode)	1.00	1.00 – 2.23
DBB (boost mode)	0.77	1.54 – 2.61
DBU-SC	1.83	1.83
DSCHB	1.42	1.42
RS-DSCHB	1.42	1.42

optimum (theoretical) voltage of the DC source (V_{dc}) of each topology to produce the rated output AC voltage mentioned in Table 2, and the DC-link voltage of the half-bridge (which may be the same as V_{dc} or different, depending on topology), both provided in per unit (p.u.) considering the magnitude of the AC voltage (V_m) as the base value.

As previously mentioned, considering the implementation with MOSFETs, the normalized conduction losses to the conduction losses of the conventional inverter are estimated using the following equation:

$$\frac{P_c}{P_{c-conv}} = \left(\frac{I_{rms}}{I_{rms-conv}}\right)^2 \tag{18}$$

where: I_{rms} and $I_{rms-conv}$ are the RMS currents of the analyzed topology and conventional inverter, respectively.

In the above equation, it was assumed that the MOSFET on-state resistances in the 1st and 3rd quadrants (i.e., for the direct and reverse current paths) are the same, while the conduction losses occurring in the body diodes during dead time are neglected (i.e., dead time was considered less than 1% of the switching time).

In the analysis of switching loss analysis, it was assumed that the switching frequency is constant for all topologies, whereas the total switching energy of the MOSFET was considered directly proportional to the voltage and current handled by the transistor at the switching instant [82]. Moreover, no switching losses occur in the SiC/GaN body diode. Therefore, the normalized switching losses relative to the switching losses of the conventional inverter are estimated as follows:

$$\frac{P_{sw}}{P_{sw-conv}} = \frac{1}{n}\sum_{k=1}^{n}\left(\frac{V_s(k)}{V_{s-conv}(k)} \cdot \frac{I_s(k)}{I_{s-conv}(k)}\right) \tag{19}$$

TABLE 6. Analysis of conduction and switching losses.

Topology	Conduction Losses (p.u.) $\frac{P_c}{P_{c-conv}}$	Switching Losses (p.u.) $\frac{P_{sw}}{P_{sw-conv}}$
Conventional	1	1
DBU	1.43	1.46
DBO	3.89	2.78
DBB (buck mode)	3.66	3.34
DBB (boost mode)	9.46	6.63
DBU-SC	3.10	3.10
DSCHB	1.99	2.41
RS-DSCHB	1.49	1.71

TABLE 7. Main inverter parameters used simulation and experimental validations.

Parameter description	Conventional H-bridge inverter	DBU inverter
Rated output active power	1kW	
DC input voltage	450V	
Output RMS voltage	230V	
Filter Capacitor	4.4μF	-
Power decoupling capacitors	-	$C_{d1} = C_{d2} =$ 60μF
Switching frequency	50 kHz	
Filter Inductors	L1 = L2 = 280μH	
MOSFETs type (SiC)	C3M0120090J	

TABLE 8. Comparative analysis of inverter losses (simulation and experiment).

Topology	Losses (simulation) [W]					Total losses (exp) [W]
	Cond.	Sw.	Cond.+Sw.	Misc.*	Total	
Conv.	8.39	3.04	11.43	11.03	22.46	24.08
DBU	11.44	3.2	14.64	12.79	27.43	29.28

*Additional losses occurring in snubbers, output inductors, decoupling capacitors.

TABLE 9. DBU inverter normalised losses (simulation and calculation).

	DBU Conduction Losses (p.u.) $\frac{P_c}{P_{c-conv}}$	DBU Switching Losses (p.u.) $\frac{P_{sw}}{P_{sw-conv}}$
Simulation	1.36	1.05
Calculation	1.43	1.19

where: V_s, V_{s-conv}, I_s, I_{s-conv} are the voltages and currents of the analyzed topology and conventional inverter, respectively, at switching instant k, and n is the total number of commutations during one period of the output voltage.

Based on the above calculation procedure, the conduction and switching losses for the analyzed topologies are listed in Table 6. Note that the two loss components are normalized to different factors; therefore, their summation does not reflect a value corresponding to the total losses. As shown, the DBU has the smallest losses, whereas the RS-DSCHB topology follows closely. As expected, DBB is the topology with the highest losses as it is configured to accept a wider input voltage variation at the expense of lower switch utilization.

As the above analysis was based on a simplified calculation procedure, the conventional and DBU topologies were further investigated using computer simulations and experiments based on the procedure described in [55]. The main parameters used in both the simulation and the experiment are listed in Table 7. In the experiment, the total losses of the SiC inverter were measured using a precise power analyzer (Yokogawa WT-1806).

Table 8 provides a comparison of the simulation and experimental results for losses in both topologies. It should be noted that while in the simulation, the various loss components (i.e., switching and conduction losses of semiconductors, snubbers, inductors, and capacitors) can be estimated, in the experimental analysis, only the overall inverter losses could be measured.

The results show that the total losses in the simulation are close to the experimental ones, indicating that the simulation model is accurate enough to be used as a reference and to compare the conduction and switching losses from the simulation with the previously calculated values. Table 9 displays the switching and conduction losses of the DBU inverter, normalized to the losses of the conventional inverter, obtained from the simulations and calculations. The similar values obtained by both methods suggest that the calculation accuracy is also maintained for the topologies listed in Table 6.

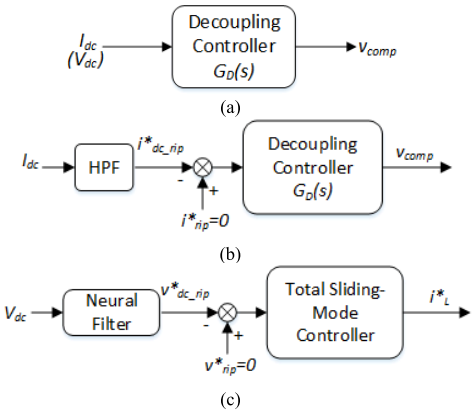

FIGURE 9. Approaches for power decoupling control: (a) PR controller (b) HPF (c) Neural filter.

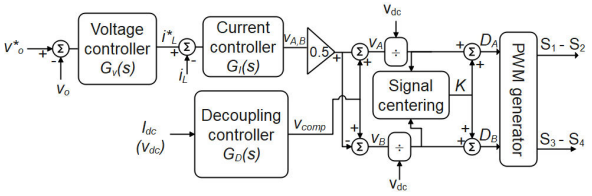

FIGURE 10. DBU inverter control with power decoupling loop [18].

IV. APD CONTROL METHODS FOR DIFFERENTIAL INVERTERS

The literature presents various control methods for the analyzed differential inverters, which can operate either autonomously with linear and nonlinear loads or grid-connected, as shown in Table 1. Control techniques share a common approach to combine output voltage/current control and decoupling control. Typically, there are two main control loops: one that handles the differential-mode (DM) component (conventional H-bridge inverter control) and the other that handles the common-mode (CM) component (decoupling control).

The power decoupling control loop relies on feeding ripple information (which can be extracted from either the DC-link voltage or DC-link current) to a decoupling controller. Based on ripple information, the decoupling controller must autonomously generate a compensation voltage v_{comp}. Several methods have been used for ripple extraction. For example, in [18], a multi-resonant controller tuned at the 2^{nd}, 4^{th} and 6^{th} order was used to extract the low-frequency ripple, as shown in Fig. 9(a). Another approach in [50] uses a high-pass filter (HPF) to extract the ripple current i_{dc_rip} from the dc link current I_{dc}. The ripple current i_{dc_rip} is then compared with the zero reference (desired ripple voltage), from which the error is fed into the proportional resonant (PR) controller to regulate the error to zero. The decoupling controller transfer function is given by (20),

$$G_d(s) = \sum_{j=2,4,6} \frac{2k_{jD}\omega_j}{s^2 + \omega_j^2} \tag{20}$$

where k_{jD} is the gain of the corresponding j^{th} component and ω_j is the pulsation frequency.

A neural filter was adopted in [66] for dc-link voltage ripple extraction and was shown to have a better dynamic response (faster settling time) than a low-pass filter. The voltage ripple is then compared to a zero-reference voltage, and the output is fed to a robust nonlinear total sliding mode controller to generate the desired inductor reference current. The advantages of the sliding mode controller are that it is robust to external disturbances and insensitive to parameter variations [83]. Ripple extraction using a high-pass filter and neural network are shown in Fig. 9(b) and Fig. 9(c), respectively.

One of the control systems first proposed in [18] for a DBU inverter operating in autonomous mode is shown in Fig. 10. The DM control loop consists of an outer voltage controller that generates the inverter current reference i_L^* to constrain the output voltage to follow the sinusoidal reference v_o^*. The error signal between the output current of the inverter i_L and the reference current i_L^* is fed to the inner current controller to generate the reference voltage, which is subsequently used to generate the duty cycles. Both controllers are implemented using PR structures, which provide a high gain around the natural resonant frequency and can be implemented in a natural reference frame [84]. Power decoupling is achieved by an additional controller composed of multi-resonant controllers tuned to amplify unwanted even harmonics (2^{nd}, 4^{th} and 6^{th} mainly) [51]. As highlighted in Fig. 10, the decoupling controller requires measuring the DC current (I_{dc}) or, in an improved version, the DC voltage (V_{dc}) [53].

The reference voltages for the two inverter arms used to generate the duty cycles are obtained by summing the differential output voltage (v_{AB}) with the CM output signal of the decoupling controller (v_{comp}). Before applying the duty cycles to the PWM generator, the signals are centered to avoid asymmetric saturation caused by the even harmonics present in these signals.

Another control approach for autonomous operation of the DBU inverter is shown in Fig. 11, which consists of two distinct parallel loops: the DM and CM loops. The DM loop consists of a PR controller structure with resonances tuned at ω and 3ω for output voltage regulation with minimum distortion. On the other hand, the CM loop is used to achieve active power decoupling. The HPF is used to extract the DC current ripple i_{dc_rip} from the DC-link current. The DC-link voltage ripple v_{dc_rip}, is then computed from the integration of i_{dc_rip}. The DC current ripple is regulated by first comparing the generated DC link voltage ripple to a zero reference before feeding the error to a PR controller. The PR controller structure is tuned to have resonances at 2ω and 4ω to remove the 2^{nd} and 4^{th} order harmonics in the DC-link current. The same controller structure can be modified to operate in grid mode as in [35]. In grid mode, the CM loop is changed to satisfy the control objective of regulating the grid current. However, additional damping may be required for both DM and CM loops, as discussed in Section IV. As time progresses, differential inverters may experience capacitor mismatches, which may degrade inverter performance owing to the additional harmonics introduced by the mismatch. To achieve good decoupling performance in the case of capacitance mismatch, the control scheme in Fig. 11 was modified in [79] for the grid-connected mode to include harmonic compensation at ω, 2ω, 3ω, and 4ω in both the CM and DM loops.

To address the nonlinearity of the DBO and DBB inverters, a feedback linearization approach is applied in [50] to a generalized half-bridge of the differential inverter. The control algorithm developed using this method has the advantage of being generalized, that is, it can be applied to all differential inverters with minor changes. The control system shown in Fig. 12 consists of a cascaded voltage and current control loop. The outer loop voltage controller generates the inductor reference current i_L^* and the inner current controller generates the duty cycle d_1. A PI and a multi-resonant controller tuned at ω, 3ω, 5ω is used to compensate for odd harmonics in the decoupling capacitors. The duty cycles can be calculated for the average model of differential single-phase inverters as follows [50]:

$$\begin{cases} d_x = \dfrac{Lsi_{L1} + v'_{Lv1}}{v_{HB-A}} & \text{Buck and buck-boost} \\ d_x = \dfrac{v'_{Lv1} - Lsi_{L1}}{v_{HB-A}} & \text{Boost} \end{cases} \tag{21}$$

where: v_{HB-A} is the voltage across the leg of the half-bridge and v'_{Lv1} is the voltage on the low-side switch.

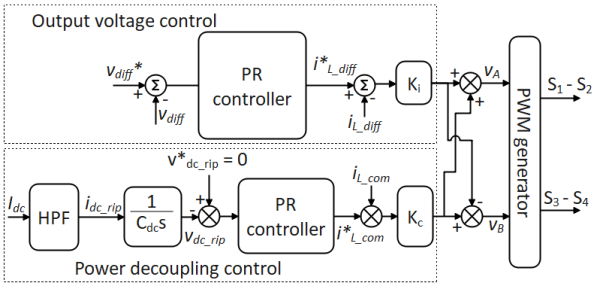

FIGURE 11. Power decoupling control for autonomous operation [50].

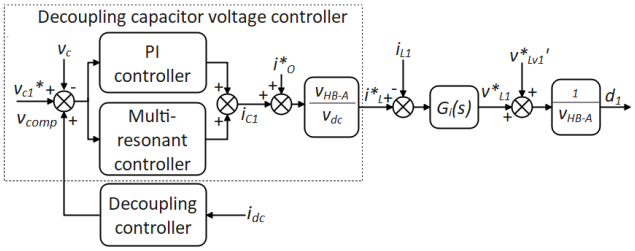

FIGURE 12. Generalized power decoupling control [50].

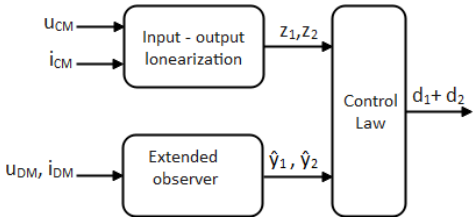

FIGURE 13. Power decoupling control [85].

A recent study proposed a control scheme based on a nonlinear power decoupling control scheme for a single-phase differential grid-tied inverter [85]. A nonlinear periodic time-varying system is transformed into a nonlinear time-invariant system using input-output linearization (IOL) coordinate transformation, which simplifies the controller design. IOL has been extensively used in the literature [86], [87], [88] and involves the use of an input-output relationship of the nonlinear system to linearize the system by transforming the inputs and outputs into a new coordinate system. A block diagram of the power decoupling scheme is shown in Fig. 13. IOL mapping transforms the system common-mode state variables u_{CM} and i_{CM} into new variables z_1 and z_2 to characterize the system. The purpose of the extended observer is to estimate the second-order ripple power that must be decoupled from the DC-link current. It improves the accuracy and reliability of state estimation by providing robust performance, even in the presence of uncertainties in the system parameters [89], [90]. The outputs $\hat{y}_1$ and $\hat{y}_2$ are extended observer estimated state variables. The control law is a function defined to ensure system stability and accurate tracking of the reference. It maps the state of the system and

the desired behavior to the control inputs, which are required to drive the system towards the desired behavior [91], [92]. The outputs d_1, d_2 are the duty cycles of the upper switches, S_1 and S_3 respectively.

A. DAMPING IN SINGLE-PHASE INVERTER

In single-phase grid-connected inverters, inductive-capacitive-inductive (LCL) filters are widely used because of their better filtering of PWM switching harmonics compared to simple inductive filters [93]. However, from a control perspective, LCL filters are more complex. They introduce a pair of system poles on the stability boundary of the closed loop, which create resonance between the filter elements [94], [95]. This resonance must be damped to achieve effective stability. Damping can be achieved either through a passive solution (i.e., adding a resistive component in parallel or in series with the filter components) or through active damping. Digitally implemented control loops have inherent modulation and computation delays that can affect the stability of the active damping loop [96], [97], [98]. Although passive damping is easy to implement, it introduces losses in the inverter [99]. Therefore, active damping methods are preferable. An overview of active damping methods is provided in [100]. The voltage and current of the capacitor within the filter can be used to achieve active damping. The decoupling capacitors of the differential inverter, which are also part of the output filter, are sufficiently large to provide ripple power processing; however, this causes the resonance frequency to be lower than that of a conventional H-bridge inverter. If the grid current is fed back to the control loop and a time delay of 1.5 T_s is considered, active damping is required if $f_r < f_s/6$ [79], where T_s is the sampling period of the controller, f_r is the resonance frequency, and f_s is the sampling frequency. Active damping for differential single-phase inverters is typically implemented separately for HB-A and HB-B [35], [79]. A virtual resistor parallel to the filter capacitor was emulated using the capacitor voltage feedback in [52] for a differential buck inverter. A filter capacitor proportional current feedback loop was implemented to emulate the virtual resistor in parallel to the filter capacitor in [35], [96], and [101]. However, this method requires measurement of the filter current, which increases the sensor count. To reduce the cost and sensor count, control techniques that rely on observations rather than measurements have been proposed. The filter capacitor current is estimated in [102] using a discrete-time full-state Luenberger observer. In [103], an extended state observer is used, which does not require the capacitor current or grid voltage to achieve active damping.

V. OPEN RESEARCH CHALLENGES

Over the last decade, research in the field of single-phase inverters has gained significant attention, mainly driven by the need to develop more efficient, reliable, and cost-effective applications. However, despite recent advancements in both control and hardware solutions, the adoption of high-speed switches (i.e., SiC/GaN semiconductors) and the necessity to implement advanced control techniques have introduced new technical challenges. One significant issue related to migration to new technologies is system lifespan extension. Specifically, in PV applications, improving the reliability of inverters is crucial for reducing the current disparity between their lifespan (typically 10-15 years) and that of PV panels (20-25 years). The goal is to extend the inverter lifespan to match that of the PV panels. Consequently, the present study focuses on the latest single-phase inverter topologies that prioritize a minimalist hardware design for active power decoupling purposes, with the use of highly reliable components, particularly film capacitors. Based on our analysis, some key factors that should be given priority in future research on highly reliable single-phase inverters are as follows:

- A deeper understanding of how single-phase inverter topologies with APD schemes, which use a minimum number of semiconductors and result in slightly higher voltage and current stress (as documented in this paper), can maintain or even enhance reliability compared with traditional topologies. Combining reduced switch count topologies and the use of wide-bandgap semiconductors may prove to be an effective design approach.
- Developing advanced control algorithms that can effectively handle the high switching frequency of modern wide-bandgap transistors, which have now reached MHz frequencies, is a crucial task. Under such circumstances, methods that do not rely on PWM modulators while maintaining a constant frequency may prove to be the optimal solution [104]. Moreover, as the switching frequency increases, the issue of leakage current becomes increasingly significant, particularly in PV applications.
- Continuing research on control solutions for grid integration and islanded operation under nonlinear operating conditions (e.g., distorted grid voltage and nonlinear loads), with a focus on improving power quality, ensuring compliance with grid codes, and facilitating seamless transitions between grid-connected and islanded operations in microgrid systems.
- Analyzing how the APD circuit influences ancillary services, such inverters must provide. For example, one challenge is related to low-voltage ride-through capability, which is imposed in many grid codes today for grid-connected inverters. With a reduction in the DC capacitance, the APD-based inverters have less energy stored in the DC link to support riding through grid voltage sags. Further research is required to provide solutions to this issue.

VI. CONCLUSION

This survey paper presented single-phase differential topologies that have been implemented in the literature to achieve active power decoupling (APD). Allowing the APD without

increasing the hardware complexity of the inverter, that is, no extra semiconductor devices are required, poses a considerable practical interest in terms of lowering cost and improving reliability. Therefore, the current study analyzed various differential inverters proposed in the literature (divided into three main classes: buck, boost, and buck-boost) in terms of switch voltage and current stresses, switch utilization, and losses. A unified mathematical description of each topology was also provided, allowing an easier evaluation of the inverters' operational limits under different parameters. Furthermore, the most common control strategies were discussed, and the main idea was to autonomously generate the compensation voltage for the effective decoupling of the oscillating power component. This minimizes the dependency of the control method on the system parameters. Based on these factors, the main conclusions of this study can be summarized as follows:

- From the point of view of switch utilization and voltage/current stress, the differential buck (DBU) inverter provides optimal performance in the class of topologies operating in buck mode, while having only a slight efficiency drop (0.5%) compared to the conventional H-bridge inverter.
- By lowering the input voltage, boost inverter topologies are inherently subjected to a higher voltage/current stress; thus, their efficiency is affected accordingly. However, a differential boost inverter may have merits in relatively low-power applications, where the single-stage boost feature represents the weight factor.
- By affecting the voltage and current stresses of semiconductor devices, decoupling capacitors are typically sized to ensure minimum inverter losses while maintaining the operational limits imposed by the application (e.g., input voltage limits). As proven by the presented results and reported in the literature, the optimal value of decoupling capacitors was approximately 1 per unit, or 60μF for a 1kW/230V inverter.
- On the control side, the analyzed inverters require an additional APD control loop, which only slightly increases the control complexity and, in the most recent developments (at least for DBU), can be implemented without additional current or voltage sensors, as compared to traditional inverters.

Overall, the choice of inverter topology depends on the requirements of the application, and designers must therefore find a balance between the cost, efficiency, and performance. Finally, further research that can lead to the development of cost-effective and more reliable single-phase inverter topologies that meet the application requirements of modern power electronics has been emphasized through an open research challenge.

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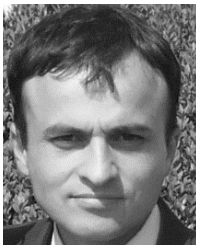
RONALD MUSONA was born in Harare, Zimbabwe. He received the B.Tech. degree (Hons.) in electronic engineering from the Harare Institute of Technology, Zimbabwe, in 2017, and the master's degree in advanced electrical systems from the Transilvania University of Brasov, Romania, in 2022, where he is currently pursuing the Ph.D. degree with the Department of Electrical Engineering and Applied Physics. He was a recipient of the Transilvania Academica Scholarship, in 2020. His research interests include power semiconductor devices and the control of power electronic converters for renewable energy sources.



IOAN SERBAN (Member, IEEE) was born in Romania, in 1981. He received the B.Sc. and Ph.D. degrees in electrical engineering from the Transilvania University of Brasov, Romania, in 2004 and 2008, respectively. He is currently a Full Professor with the Department of Electrical Engineering and Applied Physics, Faculty of Electrical Engineering and Computers Science, Transilvania University of Brasov. His research interests include power converters for interfacing renewable energy sources and energy storage systems for grid and microgrid applications. He was a recipient of the 2015 *IET Renewable Power Generation* Premium Award.